Maulana Abul Kalam Azad University of Technology, West Bengal

(Formerly West Bengal University of Technology)

Syllabus for M. Tech in Microelectronics and VLSI Technology(MVD)

(Applicable from the academic session 2019-2020)

PGMVD-101: Advanced Engineering Mathematics

[Sem – 1] 4(L) (40 Lectures) CREDIT-4

Transforms: Laplace, Fourier & Z-Transform :

Numerical Methods:

Graph Theory:

- **Introduction to Graph Theory: Definitions and Examples, Unidirected abd directed graphs, Complete graph,**
  Bipartite graphs, Trees.
- **Connectivity: Trees and Forests, biconnectivity, triconnectivity.**
- **Colouring: Cliques, Independent sets, chromatic partition.**
- **Planarity: Definitions, properties olouring.**
- **Matching: Maximum & minimum matching.**
- **Isomorphism:**

PGMVD-102: Physics of VLSI Devices

[Sem -1] 3 (L) (40 lectures)

Pre-requisite: Knowledge of basic physics of Semiconductors, Junctions and Devices - diodes, BJTs, FETs, MOS structures.

Principal Objective:

- To make the student conversant with the VLSI chip; In this context the importance of the Physics of the devices that make up the chip are to be highlighted.
- The fundamental Physics of the the Devices, with special emphasis on the MOSFET should be explained.
- The effects of scaling of device dimensions for inclusion in the VLSI chip are to be enumerated and analysed.
- Finally the methods used to overcome the limitations in the context of the devices as they appear in the VLSI chip are to be included.

Module – 1: Introduction to VLSI Design:

What is Integrated Circuit (IC)? History of IC development, Moore's Law, Different types of IC chips; Digital, Analog & Mixed signal ICs; Different Domains of VLSI design; Discussion on VLSI design fundamentals.

[Learning Outcome:

- Student will be familiar with the genesis of VLSI design.
- Student will be able to understand and explain the different Design domains and draw the Y-chart.
- Student must be able to draw the Flow-chart for VLSI design steps and explain the importance of each step.]

Module – 2: (Recapitulation and Orientation):

Discussion on properties of semiconductors in connection with the study of Physics of Junctions; Metal-metal junction, metal-semiconductor junction (Ohmic & Schottky); Bipolar Junction Transistor.

[Learning Outcome:

- The basic concept of the student in the pre-requisite to be tested through diagnostic test based on the ability of the student to calculate Fermi energy, charge concentration in the valence & conduction bands, etc.
- Student must be able to locate the Fermi energy in extrinsic semiconductors, define and calculate Work function etc.

- Student must be able to draw band-diagrams in systems in thermal equilibrium and dynamic equilibrium.
- Student must have a clear concept of effective mass, E-k diagram, direct & indirect band-gap semiconductors and their application areas.
- Student must be able to appreciate the role of Silicon in VLSI chips.]

Module -3: Field Effect Transistors & MOS:

What is Transverse field effect & how it leads to channel modulation? Different modes of channel isolation (in brief); Two Terminal MOS Structure: Flat-band voltage, Potential balance & charge balance, Effect of Gate-substrate voltage on surface condition, Inversion, Small signal capacitance; Poisson's equation for Depletion approximation model.

[Learning Outcome:

- Student will be able to explain Transverse field effect on channel modulation in Channel isolated Voltage controlled devices and name the different categories.
- Student must be able to draw band-diagrams and explain the phenomenon of channel inversion.
- Student must be able to differentiate between ideal and real MOSFETS and calculate their Threshold voltages.
- Student must acquire the ability to understand the role of MOSFET as a Capacitance.
- Student must be able to explain the variation of MOS capacitance with Gate voltage.
- Student will be able to solve one-dimensional Poisson's equation with Depletion approximation and calculate the depletion charge in the channel.]

Module – 4: Three Terminal MOS Structure:

Body effect, Regions of inversion, Pinch-off voltage; Concept of strong & weak inversion.

[Learning Outcome:

- Student will understand the importance of Body effect.
- Student will be able to calculate the change in Threshold voltage due to Body effect.]

Module – 5: Four Terminal MOS Transistor:

Current-voltage characteristic of MOSFET; Regions of operation; Solution of Poisson's equation for general channel charge model; regions of inversion - strong inversion, weak inversion, moderate inversion; Enhancement and depletion type MOSFETs. DC and AC quivalent circuit of MOSFET]

[Learning Outcome:

- Student must be able to understand the working of a complete MOSFET.
- Student must be able to identify the saturation and non-saturation regions and explain their applicabilities.
- Student must be able to solve the general Poisson's equantion in one-dimensions where both depletion and mobile channel charges are included.
- Student will be able to derive current-voltage relation from drift-diffusion equation and also from simple circuit assumptions that lead to the practical I-V relation.
- Student will be able to calculate inversion charge.
- Student will be able to draw the DC and AC equivalent circuits and hence define the different MOSFET circuit parameters like conductances, transconductances and capacitances.]

Module – 6: Small Channel Effects:

Channel length modulation, Drain induced barrier lowering, Hot electron effect & Voltage saturation effects; Effect on SCEs on MOSFET performance; Different strategies of scaling, and their relative merits & demerits; Effects of thin oxides and high doping; Sub threshold regions; Advanced MOS devices; SOC, Gate-Engineering, Multi-Gate MOSFETs; Doping Engineering, Material Engineering etc.

[Learning Outcome:

- Student must understand the different Short Channel Effects and appreciate their role in limiting the performance of the MOS.
- Student must be able to make choice of appropriate mode of scaling down as per requirement.
- Student must be able to explain the different methods of overcoming short channel effects.]

Module – 7: CMOS as Mainstay of VLSI chips:

CMOS Performance Factors: Basic CMOS circuit elements; parasitic elements; sensitivity of CMOS delay to device parameters;.

[Learning Outcome:

- Student must be able to assess the different performance parameters of a VLSI chip and comment on how to optimise the performance.
- Student will be able to calculate the energy dissipated per cycle and comment on energy requirement if speed of operation increases.
- Student must be able to identify the different regions of operation of a CMOS inverter and calculate Noise margin.

- Student must be able to identify the different parasitic components and estimate their effects on performance.]

Assignment:

Open book problem solving to familiarise the student with different theories and relations. Extension of solved problems and new problems.

Text:

1. The MOS Transistor (second edition) Yannis Tsividis (Oxford)
2. Fundamentals of Modern VLSI Devices by Yuan Taur & Tak H. Ning (Cambridge)

Reference:

1. CMOS Analog Circuit Design (second edition) Phillip E. Allen and Douglas R. Holberg (Oxford)

Additional Learning Materials:

1. Presentations prepared by self.
2. NPTEL lectures & certification modules.

PGMVD-103 :Processor Architecture & SOC Design
Sem-1 4(L) (40 Lecture)

Prerequisite:
Digital Electronics and logic design with a thorough knowledge about state machine design**.** Familiarization with assembly language programming. Synthesis/design of simple data paths and controllers. Interfacing - DAC, ADC, keyboard-display modules, etc. Development kits as well as Microprocessors / PCs / FPGA boards may be used for the laboratory, along with design/simulation tools as and when necessary.

Course Objectives:
i) Student should learn processor architecture and how to enhance performance of the processor
ii) Student should learn High Performance Computing
iii) Student should learn SoC Design
iii) Student should learn Embedded system
iv) Student should FPGA (Field Programmable Gate Array)

1**. Processor Architecture**: (4L)
a) Instruction Set Architecture: Instructions & Addressing, Procedures and Data, Assembly Language Programmes, Instruction Set Variations.
b) The Arithmetic/ Logic Unit: Number Representation, Adders and Simple ALUs, Multipliers and Dividers, Floating-Point Architecture.

2. Performance Enhancement of Processor by Pipelining: (10L)
a) Basic idea to enhance the performance of a processor, Concept of Pipelining, Pipeline performance, various hazard in pipeline, methods to solve the hazards.(4L)
b) Pipeline performance measurement parameters- speedup, efficiency, throughput, classification of pipeline processor, pipeline structure of CPU, examples from design of arithmetic pipeline- floating point adder, Multifunction pipeline, reservation table, Dynamic pipeline. (4L)
c)Vector Processing: a) Characteristics of vector processing, vector instructions, differences between scalar and vector processing with example, Pipeline chaining. (2L)

3. High Performance Computing:(6L)
a) Performance measurement parameters – MIPS, MFLOPS, SPEC rating, CPI etc., introduction to high performance computing – Overview, Flynn's classification – SISD, SIMD, MISD, MIMD. (2L)
b) SIMD Array processors: SIMD computer organization, Masking and Data-Routing Mechanisms, Inter PE Communication, SIMD Inter Connection Networks, Loosely Coupled and Tightly Coupled Multiprocessors.(4L)

4.SOC Architecture and Design: (6L)
a) Concept of SOC, Basic system -on-chip model, SOC vs processor on chip, Processor types, SOC interconnect.
b) SOC design issues: SOC architecture, Reconfigurable, on-chip bus
c) SOC Design Flow: Introduction, SOC design, SOC Co-design flow, SOC Verification and Testing.

5. Embedded System and its Architecture:(8L)
a) Why embedded system, Definition of Embedded system, Example of embedded systems, architecture of embedded systems with some example.
b) Classification of Embedded system, Co-design of Embedded system, Embedded System Development cycle, Processor interfacing.

c) Embedded System Design Issues: i) Hardware issues (Processor, Memory, Peripherals) , ii) Software issues (Programming Languages, Time Criticality, RTOS) and iii) Testing & Debugging issues (Testing Phase, Testing Tools, Software and Hardware Testing Techniques.
d) Embedded system Design Challenges: Design goal, key design challenges like performance, size, power, unit cost and NRE cost, Time to market etc.

6. FPGA (Field Programmable Gate Array) and Hardware Description Languages: (6L)
a) Needs of FPGA, Definition, Classification, Architecture, Difference between ASIC and FPGA, Synthesis on FPGA, Downloading bit stream on FPGA. (4L)
b) Design and testing of digital circuit by HDL(Hardware Describption Languages). (2L)

Course Outcomes

- Understanding computer arithmetic.
- Understanding the functional units of the processor such as the register, ALU, T&C unit Understanding addressing modes, instructions sets
- Understanding the systems topics: single-cycle (MIPS), multi-cycle (MIPS), parallel, pipelined, superscalar, and RISC/CISC architectures, SISD, MIMD, SIMD, MISD etc
- Design trade-offs in constructing a computer processor including memory.
- To be able to work with assembly language & Embedded-C programming.
- To be able to design of digital logic circuits and apply to computer organization.

Books:

1. Hamacher, Vranesic, Zaky, *Computer Organization* (McGraw Hill)
2. Hwang & Briggs, *Computer Architecture & Parallel Processing* (TMH)
3. Raj Kamal ,*Embedded SystemArchitecture, Programming and Design* (TMH)
4. Tien-Fu Chen ,*Overview of SOC architecture design*, (National Chung Cheng University)
5. Wayne Wolf, *FPGA-Based System Design* (Pearson)

Reference Books:

1. Hwang, *Advanced Computer Architecture* ,(TMH)
2. Patterson & Hennessy, *Computer Organization & design,* (Morgan Kaufmann)
3. J P Hayes ,*Computer Architecture & Organization* ,(McGraw Hill))
4. Stalling ,*Computer organization and architecture, designing for performence* ,(PHI)
5. Antonakos , *An Introduction to intel family of Microprocessors* ,(Pearson)
6. Flynn *, Computer Architecture* ,(Narosa)
7. Tammy Noergaard *, Embedded Systems Architecture – a comprehensive guide for engineers and programmer*s, (Elsevier)
8. David A. Patterson and John L. Hennessy, Computer Organization and Design
9.Carl Hamachar, Zvonco Vranesic and Safwat Zaky ,*The Hardware/Software Interface*, Elsevier.
10. William Stallings, *Computer Architecture and Organization*, McGraw Hill.
11. Vincent P. Heuring and Harry F. Jordan, *Computer Organization and Architecture: Designing for Performance*, (Pearson Education).

PGMVD-104 : Microelectronics Technology 4(L) (40 lectures)

Module-1: Introduction to Microelectronics Technology

Domain Overview:
Concepts to development of IC, Level of Integrations; Different types of Integrated circuits; Silicon as a material of choice for VLSI chip, Discussion on fabrication process fundamentals. 4L

Module – 2: Recapitulation and Orientation
Brief discussion on crystalline Properties of semiconductor in connection with the growth of Si as a substrate material, Si Ingots and wafer, Studies on properties PN Junctions; Metal-metal junction, metal-semiconductor junction (Ohmic & Schottky); 6L

Module- 3: Cleaning and Etching
Wafer Cleaning as a unit Process, Surface Contaminations, Cleaning methods : Solvent method, Pirhanah Cleaning & RCA cleaning, Concept of Clean room
(Laboratory Practices under PGMVD-191: Cleaning of p-type & n-type Si-wafer by solvent method, Piranha Cleaning & RCA cleaning) 4L
Etching – Introduction to Etch Process, Types of Etching, Issues in Etching, Basic Mechanisms of Etching process, Etch Parameters; Isotropic and Anisotropic etching. Bias and Degree of Anisotropy, Reactive Ion Etching, selective etchant for different subject. 4L

Module 4 : Oxidation
Introduction to Oxidation Process, Properties and Function of Oxide layer, Growth mechanism and kinetics of Oxidation, Oxidation Techniques and systems, growth and properties of dry and and wet oxide, Oxide properties, Oxide induced defects, characteristics of oxide films, Application of thermal oxide and CVD oxide; Dopant distribution, quality of oxide layer, Local Oxidation (LOCOS);
(Laboratory Practices under PGMVD-191: Fabrication of MOS capacitor) 8L

Future plan: Fabrication of capacitor

Module 5 : Ion implantation
Solid State Diffusion and Diffusion Vs modern method of Dopant incorporation –
Ion implantation – Range theory, Equipments, Annealing, high energy implantation

Module 6: Lithography
Introduction to Lithography, Optical Lithography: Concept of lithography room, Exposure tools, Masks, Photo resists and Pattern Transfer 6L

Module 7: Metallization
Introduction, Different types of metallisation : physical vapour deposition uses, sputtering deposition , Aluminium Metallization, Junction spiking,, Electromigration, Damascene and Dual damascene technology, Salicide technology 4L
Laboratory Practices under PGMVD-191 Learning Metallisation process (PVD) by using Thermal evaporation and Electron beam gun)

Module 8:
VLSI Process integration for making a particular Device (MOSFET) 2L

Text Book:

- Sze, S.M , Wiley, 1985*, Semiconductor Devices: Physics and Technology*,

- Campbell ,*The Science and Engineering of Microelectronic Fabrication*,Oxford University Press
-

Reference Book:

- Morgan, D.V., and Board, K , *An Introduction to Semiconductor Microtechnology*
- The National Technology Roadmap for Semiconductors , Notes: Semiconductors Industry Association, SIA, 1994
- Sze, S.M. , *Electrical and Electronic Engineering Series VLSI Technology*, Mcgraw-Hill International Editions
-

Assignment: Open book problems are given to solve to familiarise the students with different theories and relations. Extension of Problems and are be appreciated.

Additional Material:
Presentation prepared by myself

NPTEL Lectures and Certification modules,

Programme Outcome:

- Student must be able to appreciate the role of material Silicon in VLSI chips.
- Student must have a clear concept of the Unit Processes and their specific application area.
- Student must be able to understand the fabrication of a complete device.

Student must be able to assess the different performance parameters of the unit process of a VLSI chip and comment on how to optimise the

PGMVD-105 :Digital VLSI Circuits & Systems
[Sem–1] 3(L) 1(T) 2 (P) credit-4

Prerequisite:
Overview of CMOS VLSI fabrication, CMOS process steps; fabrication; yield; design rules for custom layout; Layout - hand layout, graphical layout, low-level language; design rule checking; stick diagrams; placement of cells; simulation of design; function generation from masks; test pattern generation; structured design methodology for VLSI; hierarchical design techniques and examples. Concept of Mask design, Mask layout, Stick diagram, Standard cell Vs Custom design,

1.Specification Methods:
Language based methods including VHDL/Verilog, hierarchical state machine descriptions such as State Charts, and Petri net based methods. Functional languages for formal verification.
(Laboratory Practises for PGMVD192: RTL description of combinational and sequential circuits using
PGMVD-102: Physics of VLSI Devices [Sem -1] 3 (L) (40 lectures)

Pre-requisite: Knowledge of basic physics of Semiconductors, Junctions and Devices - diodes, BJTs, FETs, MOS structures.

Principal Objective:

- To make the student conversant with the VLSI chip; In this context the importance of the Physics of the devices that make up the chip are to be highlighted.
- The fundamental Physics of the the Devices, with special emphasis on the MOSFET should be explained.
- The effects of scaling of device dimensions for inclusion in the VLSI chip are to be enumerated and analysed.
- Finally the methods used to overcome the limitations in the context of the devices as they appear in the VLSI chip are to be included.

Module – 1: Introduction to VLSI Design:

What is Integrated Circuit (IC)? History of IC development, Moore's Law, Different types of IC chips; Digital, Analog & Mixed signal ICs; Different Domains of VLSI design; Discussion on VLSI design fundamentals.

[Learning Outcome:

- Student will be familiar with the genesis of VLSI design.
- Student will be able to understand and explain the different Design domains and draw the Y-chart.
- Student must be able to draw the Flow-chart for VLSI design steps and explain the importance of each step.]

Module – 2: (Recapitulation and Orientation):

Discussion on properties of semiconductors in connection with the study of Physics of Junctions; Metal-metal junction, metal-semiconductor junction (Ohmic & Schottky); Bipolar Junction Transistor.

[Learning Outcome:

- The basic concept of the student in the pre-requisite to be tested through diagnostic test based on the ability of the student to calculate Fermi energy, charge concentration in the valence & conduction bands, etc.

- Student must be able to locate the Fermi energy in extrinsic semiconductors, define and calculate Work function etc.
- Student must be able to draw band-diagrams in systems in thermal equilibrium and dynamic equilibrium.
- Student must have a clear concept of effective mass, E-k diagram, direct & indirect band-gap semiconductors and their application areas.
- Student must be able to appreciate the role of Silicon in VLSI chips.]

Module -3: Field Effect Transistors & MOS:

What is Transverse field effect & how it leads to channel modulation? Different modes of channel isolation (in brief); Two Terminal MOS Structure: Flat-band voltage, Potential balance & charge balance, Effect of Gate-substrate voltage on surface condition, Inversion, Small signal capacitance; Poisson's equation for Depletion approximation model.

[Learning Outcome:

- Student will be able to explain Transverse field effect on channel modulation in Channel isolated Voltage controlled devices and name the different categories.
- Student must be able to draw band-diagrams and explain the phenomenon of channel inversion.
- Student must be able to differentiate between ideal and real MOSFETS and calculate their Threshold voltages.
- Student must acquire the ability to understand the role of MOSFET as a Capacitance.
- Student must be able to explain the variation of MOS capacitance with Gate voltage.
- Student will be able to solve one-dimensional Poisson's equation with Depletion approximation and calculate the depletion charge in the channel.]

Module – 4: Three Terminal MOS Structure:

Body effect, Regions of inversion, Pinch-off voltage; Concept of strong & weak inversion.

[Learning Outcome:

- Student will understand the importance of Body effect.
- Student will be able to calculate the change in Threshold voltage due to Body effect.]

Module – 5: Four Terminal MOS Transistor:

Current-voltage characteristic of MOSFET; Regions of operation; Solution of Poisson's equation for general channel charge model; regions of inversion - strong inversion, weak inversion, moderate inversion; Enhancement and depletion type MOSFETs. DC and AC quivalent circuit of MOSFET]

[Learning Outcome:

- Student must be able to understand the working of a complete MOSFET.
- Student must be able to identify the saturation and non-saturation regions and explain their applicabilities.
- Student must be able to solve the general Poisson's equantion in one-dimensions where both depletion and mobile channel charges are included.
- Student will be able to derive current-voltage relation from drift-diffusion equation and also from simple circuit assumptions that lead to the practical I-V relation.
- Student will be able to calculate inversion charge.

- Student will be able to draw the DC and AC equivalent circuits and hence define the different MOSFET circuit parameters like conductances, transconductances and capacitances.]

Module – 6: Small Channel Effects:

Channel length modulation, Drain induced barrier lowering, Hot electron effect & Voltage saturation effects; Effect on SCEs on MOSFET performance; Different strategies of scaling, and their relative merits & demerits; Effects of thin oxides and high doping; Sub threshold regions; Advanced MOS devices; SOC, Gate-Engineering, Multi-Gate MOSFETs; Doping Engineering, Material Engineering etc.

[Learning Outcome:

- Student must understand the different Short Channel Effects and appreciate their role in limiting the performance of the MOS.
- Student must be able to make choice of appropriate mode of scaling down as per requirement.
- Student must be able to explain the different methods of overcoming short channel effects.]

Module – 7: CMOS as Mainstay of VLSI chips:

CMOS Performance Factors: Basic CMOS circuit elements; parasitic elements; sensitivity of CMOS delay to device parameters;.

[Learning Outcome:

- Student must be able to assess the different performance parameters of a VLSI chip and comment on how to optimise the performance.
- Student will be able to calculate the energy dissipated per cycle and comment on energy requirement if speed of operation increases.
- Student must be able to identify the different regions of operation of a CMOS inverter and calculate Noise margin.
- Student must be able to identify the different parasitic components and estimate their effects on performance.]

Assignment:

Open book problem solving to familiarise the student with different theories and relations. Extension of solved problems and new problems.

Text:

3. The MOS Transistor (second edition) Yannis Tsividis (Oxford)
4. Fundamentals of Modern VLSI Devices by Yuan Taur & Tak H. Ning (Cambridge)

Reference:

2. CMOS Analog Circuit Design (second edition) Phillip E. Allen and Douglas R. Holberg (Oxford)

Additional Learning Materials:

3. Presentations prepared by self.
4. NPTEL lectures & certification modules.

2.Synthesis tools: High level synthesis; Scheduling allocation, communication and control.
(Laboratory Practises for PGMVD192: Synthesis of the RTL designs using an industry standard synthesis tool and power and timing analysis of the synthesised designs)

3.Module Generation: Finite State machines, state encoding, parameterised blocks PLA, RAM, ROM generation. Gate Level Synthesis; Binary Decision Diagrams, Logic minimisation, optimisation and retargeting.(Laboratory Practises of PGMVD-192: Simulation and Synthesis of finite state machines)

4.Layout Synthesis: Placement; simulated annealing, genetic algorithms, constructive methods. Routing;
nets, layers, Lees algorithms, cost functions, channel routing. Examples of a channel router with placement ,expansion.

5.Case Study: Synthesis of a chosen algorithm to the gate level using CAD tools.
(Laboratory Practices for PGMVD192) Case Study Lecture: Design of MSI chip using proprietary CAD system; use of circuit description language; layout considerations.
(Laboratory Practises for PGMVD 192: A complete VLSI design example : from RTL to GDSII)

6.Complex gates: Pseudo NMOS; dynamic logic; dynamic cascaded logic; domino logic; 2 and 4 phase logic; pass transistor logic. Control and timing; synchronous and asynchronous; self-timed systems; multi-phase clocks; register transfer; examples of ALU, shifters, and registers.
(Laboratory Practises for PGMVD 192: Schematic and layout creation of basic and complex gates based on different design libraries). Emerging concepts: Synchronisers and arbeiters, networks on a chip.

7.Effects of scaling circuit dimensions: Physical limits to develop fabrication. Optional extended course work for final year students, using VLSI design software to produce a chip to meet a given specification; the chip may be fabricated if the design is successful. To study the different stages in the design of integrated chip using VLSI design software. The design is to meet a given specification.

Reading List

1. Russell, G, Kinniment, D.J., Chester, E.G., and McLauchlan, M.R.*, CAD for VLSI*
Notes: Van Norstrand Rheinhold, 1985.
2. McFarland, M.C., Parker, A.C and Camposano R ,*Tutorial on High Level Synthesis*
Notes: Proc 25th ACM/IEEE Design Automation Conf pp330-336
3. Neil Weste and David Harris, *CMOS VLSI DesignA Circuits and Systems Perspective*
(3rd Edition)

PGMVD-191:Microelectronics Lab-I (Fabrication Techniques)

1. Cleaning the substrate by using Solvent Method.
   a. Glass Substrate
   b. Silicon substrate (P-type and n-type)
2. Cleaning the n-type and p-type water for further processing / Thin film deposition using following methods:-
   a. Solvent method.
   b. Piranha Method.
   c. RCA Cleaning method.
3. a. Etching of a cleaned P-type Si-wafer by using HF:HNO_3 in required Stoichiometric volume.
   b. Study the sample under compound microscope and Study illumination of the sample under UV light.
4. Study the etching rate under environmental condition:- i) Isotropic etching.
   ii) Anisotropic etching.
5. Contact metallisation on Si wafer by using Physical Vapour Deposition
   a. Ohmic contact.
   b. Schottky contact.
      i) By using electro-less method.
      ii) By using screen printing method.
      iii) By using Electroplating method.

PGMVD-192: VLSI Design - Lab-I
[Sem -1] Contact hours :3P Credit points:2

Pre-requisite: Knowledge of programming, Basic gates, Digital Circuits – Combinational & Sequential

Part-A : FPGA Based Digital Design

Software & Hardware Tools – Xilinx ISE, VIVADO, FPGA Boards

LAB – 0A: Introduction to FPGA Based Digital Design:
- Register-transfer-level abstraction
- Introduction to HDL Coding by Basic Digital Gates
- Using Xilinx ISE Pack for HDL Coding, Simulation & Synthesis

LAB – 0B: Understanding the FPGA Board
- Identifying the Board Parts
- Procedure of Bit-Stream Downloading by Basic Digital Gates
- JTAG

LAB – 1: Writing Verilog Code, Test Bench for Simulation & Synthesis
- Combinational Circuit – Multiplexer, Demultiplexer

LAB – 2: Writing Verilog Code, Test Bench for Simulation & Synthesis
- Combinational Circuit –
- Construction of Higher Level Multiplexer using Lower Level Mutiplexer
- Circuit Designing using Multiplexer

LAB – 3: Writing Verilog Code, Test Bench for Simulation & Synthesis
- Sequential Circuit –
- Flip-Flop – SR, D, JK, T

LAB – 4: Writing Verilog Code, Test Bench for Simulation & Synthesis
- Sequential Circuit –
- Counter – Up, Down, Bidirectional\

LAB – 5: Writing Verilog Code, Test Bench for Simulation & Synthesis
1. Sequential Circuit –
2. Register – Left/Right Shift Register

LAB – 6: Writing Verilog Code, Test Bench for Simulation & Synthesis
1. Sequential Circuit –
2. FSM – Melay & Moore

Part-B : FrontEnd Using Synopsys

Software – Synopsys, CentOS

LAB – 7: Writing Verilog Code, Test Bench for Simulation & Synthesis
3. ALU Design

LAB – 8: Synopsys Front End - Introduction
- Using Verilog Compiler Simulator (VCS)
- Using DVE for analyze, compile and simulate
- Using Design Vision for Synthesys & Gate Level Netlist preparation

LAB – 9: Synopsys Front End - Experiment
- Experiment with Up-Down Counter with above 3 modules
- Functionality Check
- Timing Analysis
- Power Analysis

PGMVD-201: Analog VLSI Circuits & Systems
[Sem – II] 3(L) 0T) 0(P) 3 Lectures

Pre-requisite: Knowledge of Electrical circuits and networks taught in graduate programme and knowledge of Semiconductor devices used in connection with VLSI circuits taught in semester 1.

Principal Objective:

- To make the student conversant with the difference between Analog and Digital VLSI design. In this context the importance of the CMOS as the basic unit of design is to be highlighted.
- The importance of CMOS technology and its application in fabricating MOS-based passive circuit components are to be described. Behaviour and characteristics of MOS as a switch will also be explained.
  The Analog sub-circuits are to be listed and their different structures exploiting the MOSFET are to be analysed.
- The sub-circuits to be studied are Current sources, current mirrors, Voltage references, different kinds of CMOS amplifiers. These circuits are to be explained with suitable equivalent circuits and their detailed analysis.
- The Operational Amplifier and its different sub-components utilising the basic sub-circuits are to be explored.
- Finally the basic concepts behind circuits acting as Analog-to-Digital and Digital-to-Analog converters, and Switched Capacitor circuits are to be discussed in brief.

Module -1: Analog Circuit Design:
Introduction to Analog circuit design; Difference between Digital IC and Analog IC design; CMOS as the mainstay of VLSI design; Analysis & Synthesis.

Module – 2: Different technologies of Analog VLSI – a brief overview:
Different technologies for Analog IC design; Paasive circuit components in VLSI;

Module – 3: Analog Subcircuits:
List of sub-circuits; MOS as a switch; Active load; Voltage divider; Current source & sink; Current mirror.

Module – 4: CMOS Amplifiers:
Inverters – Active load inverter, Current source load inverter, Push-pull inverter; Differential amplifiers; Cascade amplifiers, Miller effect; Output stage; Class A amplifiers.

Module – 5: **Different types of Amplifiers**:
Current Amplifiers; Class A amplifiers; Output stages - Source Followers; Push-pull Common Source amplifiers; High-gain amplifiers; Different types of Feedback amplifiers; OPAMPs.

Module – 6: Other Sub-circuits:
Comparators; AD & DA conversion; Swiched-mode circuits – principle of operation.

Assignment:
Open book problem solving to familiarise the student with different theories and relations. Extension of solved problems and new problems.

Text:

1 CMOS Analog Circuit Design (second edition) Phillip E. Allen and Douglas R. Holberg (Oxford)

Reference:

1. Weste N and Eshraghian K; Addision Wesley 1985 ,*Principles of CMOS VLSI Design*
2. Mukherjee A , 1986, *Introduction to NMOS and CMOS VlSI Systems Design* , Prentice-Hall
3. Mead and Conway, *Introduction to VLSI System*s , Notes: Addison Wesley D C & Co

Learning Outcome:

- Student must appreciate and understand the main elements of Analog VLSI design.
- Student must acquire the proficiency to analyse the analog VLSI sub-circuits and compare their relative merits and demerits that will help them to make an informed choice of the sub-circuits in designing modules.
- Hands-on training: Students must be able to use analytical tools like SPICE, PSPICE,

HSPICE and any other similar tool to synthesise the circuits and analyse them as needed for circuit simulation in Laboratory PGVLSI 296.

Additional Learning Materials:

1 Presentations prepared by self.
2 NPTEL lectures & certification modules.

PGMVD-202
Testing & Verification of Digital Systems:
Course Objectives:
i) Student should learn the concept of Testing of VLSI Design.
ii) Student should learn Various kind of Fault Models.
iii) Student should learn Fault detection methods of combinational and Sequential circuits.
iv) Student should learn various testing tools.
v) Student should learn about Design for Testability and verification of VLSI design.
Course Outcomes:
i) Be able to find the “TEST” for Combinational circuits.
ii) Be able to find the “TEST” for Sequential circuits.
iii) Be able to utilized the Various testing tools like ICE, JTAG, ISE etc.
iv) Able to design the suitable circuit for Testing.
v) Able to understand the Verification Methods.
1. Introduction: (2Hrs)
1.1 What is Testing for VLSI systems,
1.2 Importance of Testing,
1.3 Definition of Basics terms: Failure, Fault, Error, Verification etc.,
1.4 Overview of Testing Tools.
2. Fault Models: (10 Hrs)
2.1 Characteristics of Fault: Nature, Value, Extend, Duration ; Fault Models, Details of Stuck-At-Fault Model description with examples.
2.2 Bridging Faults Model: Defination, Classifications, Description with examples; Delay Fault Model.
2.3 Breaks : Inragate breaks, Signal line breaks with suitable example; Stuck-On and Stuck-Open Faults with suitable example.
2.4 Basic Concept of Fault Detection : Excitation and sensitization; Controiiability and Observability, Undetectable Faults.
2.5 Equivalent Faults, Temporary Faults, Testing Bench design for testing a design using HDL.

3. Testing Tools: (8Hrs)
3.1 Differences between Simulator and Emulator, Hardware Testing by CRO, DSO, Logic analyzer, ICE(In-Circuit-Emulator): What is ICE, Operation principle of ICE, Important Features of ICE.
3.2 JTAG:What is JTAG, Importance of JTAG Technology; Features of Boundary Scan, Principle of Boundary Scan.
3.3 Operation of Basic Boundary Scan Cell (BSC), Test process of Boundary Scan, Advantages of Boundary Scan B Features of Boundary Scan.
3.4 Important Role of FPGA for Testing a Design, How testing is done by Simulation and Synthesis for FPGA based design, Details discussion of ISE tool.
4. Fault Detection of Combinational Circuits: (6 Hrs)
4.1 Aim of Testing, Fault coverage, Test generation (Truth Table for fault and faulty circuit, Fault matrix, Minimal test set).
4.2 Path Sensitization: forward tree and backward tree; Cubical algebra for automatic generation of tests (Singular cube, Propagation D-cube, Primitive D-cube of a fault).
4.3 D-Algorithm with example, PODEM-Algorithm.
5. Fault Detection of Sequential Circuits: (8 Hrs)
5.1 Testing of Sequential circuits: general model of a synchronous sequential circuit, concept sequential circuit testing, checking experiment, checking sequence, assumptions of the sequential circuit for derivation of checking sequence, homing and distinguishing sequence.
5.2 Initial uncertainty, Uncertainty vector, Trival Uncertainty Vector, Homogeneous Uncertainty Vector, Homing tree and Homing Sequence, Distinguishing tree and Distinguishing Sequence.
5.3 Importance of Transfer Tree and Transfer Sequence with some examples, Phases of checking experiments (Initial phase, state identification phase and Transition verification phase)
5.4 Test Generation using sequential circuit structure and the state table with example.
6. Design for Testability(DFT): (2Hrs)
6.1 Adhoc Techniques, Scan-Path Technique for testable sequential circuit design, Level-Sentative Scan Design (Clocked Hazard-Free Latches and Double-Latch and Single-Latch LSSD)
7. Introduction to Verification: (4Hrs)
7.1 Design Verification: Introduction, Difference between testing and verification, Design challenges, Digital design with examples, Abstraction in design flow, Design cycle, Design and verification, Functional verification challenge, Dynamic Property Verification (DPV).
7.2 Formal Property Verification(FPV), Assertion based verification flow, Review and Discussion.

Books:
1. Parag K. Lala, An Introduction to Logic Circuit Testing, Morgan & Claypool Publishers, 2009.
2. William K Lam, Hardware Design Verication: Simulation and Formal Method-Based Approaches, Prentice Hall, March, 2005.
Reference Books:
1. Michael L. Bushnel and Vishwani D. Agrawal , Essentials of Electronic Testing -for digital, memory and mixed-signal VLSI circuits, Kluwer Academic Publishers, 2002.
2. Samiha Mourad and Yervant Zorian, Principles of Testing Electronic Systems, John Wiley & Sons,Inc, 2000.
3. pallab Dasgupta, A roadmap for Formal Property Verification, Springer, 2006.

PGMVD-202:Testing & Verification of VLSI Systems

Course Objectives:
i) Student should learn the concept of Testing of VLSI Design.
ii) Student should learn Various kind of Fault Models.
iii) Student should learn Fault detection methods of combinational and Sequential circuits.
iv) Student should learn various testing tools.
v) Student should learn about Design for Testability and verification of VLSI design.
Course Outcomes:
i) Be able to find the "TEST" for Combinational circuits.
ii) Be able to find the "TEST" for Sequential circuits.
iii) Be able to utilized the Various testing tools like ICE, JTAG, ISE etc.
iv) Able to design the suitable circuit for Testing.
v) Able to understand the Verification Methods.
1. Introduction: (2Hrs)
1.1 What is Testing for VLSI systems,
1.2 Importance of Testing,
1.3 Definition of Basics terms: Failure, Fault, Error, Verification etc.,
1.4 Overview of Testing Tools.
2. Fault Models: (10 Hrs)
2.1 Characteristics of Fault: Nature, Value, Extend, Duration ; Fault Models, Details of Stuck-At-Fault Model description with examples.
2.2 Bridging Faults Model: Defination, Classifications, Description with examples; Delay Fault Model.
2.3 Breaks : Inragate breaks, Signal line breaks with suitable example; Stuck-On and Stuck-Open Faults with suitable example.
2.4 Basic Concept of Fault Detection : Excitation and sensitization; Controiiability and Observability, Undetectable Faults.
2.5 Equivalent Faults, Temporary Faults, Testing Bench design for testing a design using HDL.
3. Testing Tools: (8Hrs)
3.1 Differences between Simulator and Emulator, Hardware Testing by CRO, DSO, Logic analyzer, ICE(In-Circuit-Emulator): What is ICE, Operation principle of ICE, Important Features of ICE.
3.2 JTAG:What is JTAG, Importance of JTAG Technology; Features of Boundary Scan, Principle of Boundary Scan.
3.3 Operation of Basic Boundary Scan Cell (BSC), Test process of Boundary Scan, Advantages of Boundary Scan B Features of Boundary Scan.
3.4 Important Role of FPGA for Testing a Design, How testing is done by Simulation and Synthesis for FPGA based design, Details discussion of ISE tool.
4. Fault Detection of Combinational Circuits: (6 Hrs)
4.1 Aim of Testing, Fault coverage, Test generation (Truth Table for fault and faulty circuit, Fault matrix, Minimal test set).
4.2 Path Sensitization: forward tree and backward tree; Cubical algebra for automatic generation of tests (Singular cube, Propagation D-cube, Primitive D-cube of a fault).
4.3 D-Algorithm with example, PODEM-Algorithm.
5. Fault Detection of Sequential Circuits: (8 Hrs)
5.1 Testing of Sequential circuits: general model of a synchronous sequential circuit, concept sequential circuit testing, checking experiment, checking sequence, assumptions of the sequential circuit for derivation of checking sequence, homing and distinguishing sequence.
5.2 Initial uncertainty, Uncertainty vector, Trival Uncertainty Vector, Homogeneous

Uncertainty Vector, Homing tree and Homing Sequence, Distinguishing tree and Distinguishing Sequence.
5.3 Importance of Transfer Tree and Transfer Sequence with some examples, Phases of checking experiments (Initial phase, state identification phase and Transition verification phase)
5.4 Test Generation using sequential circuit structure and the state table with example.
6. Design for Testability(DFT): (2Hrs)
6.1 Adhoc Techniques, Scan-Path Technique for testable sequential circuit design, Level-Sentative Scan Design (Clocked Hazard-Free Latches and Double-Latch and Single-Latch LSSD)
7. Introduction to Verification: (4Hrs)
7.1 Design Verification: Introduction, Difference between testing and verification, Design challenges, Digital design with examples, Abstraction in design flow, Design cycle, Design and verification, Functional verification challenge, Dynamic Property Verification (DPV).
7.2 Formal Property Verification(FPV), Assertion based verification flow, Review and Discussion.

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1. Parag K. Lala, An Introduction to Logic Circuit Testing, Morgan & Claypool Publishers, 2009.
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2. Samiha Mourad and Yervant Zorian, Principles of Testing Electronic Systems, John Wiley & Sons,Inc, 2000.
3. pallab Dasgupta, A roadmap for Formal Property Verification, Springer, 2006.

PGMVD 203: Digital Signal Processing and Applications
3(L) 0(T) 0(P)

I. Signals& Systems

1. Concept of Systems and Properties of linear time-invariant system**.**

- To understand different properties of LTI System. The principal objective is to understand the Linearity and Time Invariant Properties of a LTI System.
- Concept of convolution.
- Series and Parallel system

2. **Introduction to Discrete Time Signal & Systems**

- To provide an overview of discrete time signals and systems on MATLAB.
- To understand basic building blocks like adder, multiplier and delay units.
- Understanding Dirac's delta function and study the characteristics using Matlab.
- understanding unit sample, unit step and ramp functions and study using Matlab
- To analyze various properties of discrete signals and verify them on Matlab.
- Implementation of integrator, differentiator using multiplier, adder and delay.
- Z – Transform: To analyze unilateral and bilateral z transforms of various signals. Also to analyze how unilateral z transform can be used to obtain system responses with initial conditions or changing inputs.
- Bi-linear transformation:
- To find out the bi-linear relation between Z and S and to validateusing Matlab.
- Model the digital version of an analog low – pass RC circuit and study the performance.

II. Digital Signal Processing (DSP)

- Study of sampling theorem, effect of under sampling
- This experiment enables to learn how to view the analog signal using Matlab.
- How to set the amplitude, frequency and phase of the signal source.
- How to set the sampling frequency of the source such that the signal can be reconstructed. All these experiments must be done on real-life signals using Matlab/FPGA/ARM Processor.
- **Aliasing Problem**: To analyze the effect of under-sampling a signal using Matlab.
- Study of Quantization of continuous-amplitude, discrete-time analog signals

- To learn How to set the number of levels of a quantizer.
- Calculate the error involved after quantization of the signal (The principal objective of this experiment is to understand the principle of quantization error).
- Study of different types of Companding Techniques
- To understand different types of non-uniform quantization techniques
- To understand the compression and expansion process involved in companding technique using MATLAB/FPGA/ARM Processor.
- **Discrete Time Fourier Transform**
- To form a routine of discrete time Fourier transform on Matlab,
- Computer discrete time Fourier transform of various signals on Matlab.
- Analyze different application of discrete time Fourier transforms.
- **Properties Of Discrete Time Fourier Transform**

3. Discrete Fourier transform, decimation in time and decimation in frequency.

4. To study various properties of discrete time Fourier transform and verify these properties on various signals on MATLAB.

5. To form a routine of discrete Fourier transform on Matlab and find discrete Fourier transform of various signals on Matlab.

6. Analyze different properties of discrete Fourier transform.

- **Fast Fourier Transform**

4. Fast Fourier transform (FFT) algorithm and complexity analysis.

5. To analyze fast Fourier algorithms and analyze using MATLAB.

6. Architecture of DFT and FFT Processor.

- **DSP Architecture:** Different DSP Processors and their Architectures, Implementation of DSP algorithms on 16 bit , 32 bit DSP Processors like TMS320 C30 , TMS 320 C65XX series DSP Processors and on FPGAs like Xilinx Spartan 6E, Virtex 6, Artix 7 etc.
- **Digital Filter Design**

1. To design and simulate Chebychev and Butterworth filters and analyze their responses on MATLAB/ FPGA/DSP Processors.

2. Digital Filter Design and implementation on FPGA board

2 To design and simulate Infinite Impulse Response (IIR) Filters andFinite Impulse Response (FIR) filters and analyzes their responses on Matlab/FPGA board.

- **Multi-Rate Signal Processing**
- Introduction
- Why multi-rate Signal processing?
- Up Sampling , Down Sampling, rational sampling
- CIC (Cascaded Integrated comb filtering}
- **Adaptive Signal Processing.**
- Introduction
- LMS algorithm
- Adaptive filtering with DCT/ LMS
- Applications: Adaptive echo cancellation, Adaptive echo cancellation, fatal electrocardiography etc.
- **Time frequency analysis and introduction to wavelet transform.**

3 Introduction

4 Time frequency analysis

5 Limitation of Fourier transform

6 Short term Fourier transform

7 Mathematical expression of Wavelet transform and analysis

8 Wavelength transform algorithm and architecture.

9 Application of wavelet transform

- **Introduction to SIMULINK**
- **To get familiar with SIMULINK working environment**.

3 Construction of different models in SIMULINK. Simulate and observe the responses.

4 Applications to SIMULINK:To see how different tool boxes can be usedand to find various transforms on Simulink by using different tool boxes.

III. DSP Applications

1. **Implementation of DSP building blocks /functions** on MATLAB / FPGA / ARM Processor.

2.**Applications of DSP**

a. DTMF detection

b. Adaptive filters

5 LMS algorithm

6 Adaptive echo cancellation

c. Modulator/ demodulator using amplitude modulation/demodulation.

IV. Final Project / Term Paper

Course Outcome:

- The aim of this section is to understand and grasp a thorough knowledge of Signals & Systems through a series of experiments using the supplied board.)
- The aim of this section is to understand and grasp a thorough knowledge of Digital Signal Processing System
- Provides the users with familiarity of different DSP applications and their design techniques.

References: 1. Digital Signal Processing by Sanjit Kumar Mitra, Macgrow Hill Publication.

2. Digital Signal Processing by Proakis, Pearson publication

3. Digital Signal Processing by Antonio, Macgrow Hill Publication.

PGMVD-204:Advanced Micro and Nano Devices

Prerequisite :

Fundamentals of semiconductor physics and basics of p-n junctions, bipolar transistors, JFETs, MOS capacitors,

MOSFETs, CMOS, low and high frequency equivalent circuits of BJTs and MOSFETs, IC technology.

Course content:

Module-1 (14 lectures) – [Recapitulation of MOS scaling laws, Short channel effects, MOSFET models], Nano CMOS, Effects of gate oxide tunneling, Concept of EOT, high-k dielectrics, Effects of nanoscaling on MOSFET characteristics and performance, Technology trend, Advanced CMOS structures, SOI.

Module-2 (8 lectures) – Semiconductor heterojunctions; compound semiconductor and silicon-germanium

heterostuctures, superlattice, HBTs, PETs, MESFETs, advanced solar cell structures.

Module-3 (14 lectures) – Fundamental concepts of quantum structures and tunneling junctions, Nanotubes, Devices

based on quantum wells, quantum wires/nanotubes and quantum dots – HEMTs, RTDs, CNT MOSFETs, SETs,

Terahertz devices, advanced optoelectronic devices.

Module-4 (6 lectures) – Outline of nanofabrication – nanolithography, MBE, MOVPE; Introduction to molecular

electronics.

Module-5 (5 lectures)– Optical Properties, Photoconductivity, Optical absorption & transmission, Photoluminescence, Fluorescence, Phosphorescence, Electroluminescence., LEDs, laser diodes, photodetectors, solar cells.

Text Books:

Ning & Taur

B.R.Nag

S.M. Sze

Quantum Physics – A. Ghatak

Quantum Mechanics - Bransden and Joachen

Outcomes:

List of course outcomes

Overall: Familiarity with advanced structures, their relative merits and demerits, areas of application

1. Ability to learn the basic philosophy and in-depth structure of various fields of the program with a motivation to the importance of lifelong learning.

2. Students will nurture their innovative skills in formulating and solving real world problem with a robust analysis that will enhance the quality of both the students and faculties.

The students are exposed to the cutting edge technologies as prevailing across the globe. Some significant courses offered by our department towards VLSI based PG studies are Analog Design, Digital Design, Mixed Signal IC Design, VLSI Technology, VLSI Testing etc. The aforementioned subjects allow to boost up the potential of scientific and innovative research and enhances the capability to be acquainted with the present day technologies adopted in different public and private sectors.

Explain how modes of delivery of courses help in attainment of the POs

Apart from taking regular and exhaustive classes, the students are always entertained and encouraged to participate in technical prototype projects as well as inducted to real world challenges given by front end customers.

The students do participate in technical debate as well as are engaged in solving the technical assignments related to the concerned subjects. Apart from adopting the conventional way of delivering lectures, the faculties also share video lectures, PPTs, remedial classes, doubt sessions with the students.

Indicate how assessment tools used to assess the impact of delivery of course/course content contribute towards the attainment of course outcomes/programme outcomes:

The following assessment tools are practiced regularly.

(1) Approx 10 minutes are spent in each class to clarify technical queries of the students.
(2) Regular assignments and term projects are given to the students.
(3) Mid-term assessment and end semester assessments.

PGMVD205:Project Management

- Project Management-Concept & Relevance
- Project Organization, Structure of organisations and projects , distinguish between different types of organisational structure , Responsibility Assignment Matrix , roles and responsibilities of project sponsor, project manager, team members, project steering group, users ,relationship between project sponsor and manager, Project Management Functions
- Project life cycle , project life cycle phases , difference between project life cycle and extended life cycle ,sharing knowledge , benefits of conducting reviews
- Project Management Tool
- Project Network Analysis
- Schedule and resource management , project scheduling , categories and types of resources , resource smoothing and levelling, financial and cost management , budget and cost control
- Project risk management and issue management , risk management process , risk as threat and opportunity , benefits of risk management ,distinguish between a risk and an issue , escalation
- Project Appraisal
- Scope management, Product Breakdown Structure {PBS}, Work Breakdown Structure {WBS} , configuration , requirements , change control, links with configuration
- Project Quality, Describe quality management , quality planning, assurance, control and continual improvement
- Computerized Project Management

PGMVD-291:MICROELECTRONICS LAB – II(CHARACTERIZATION)

1. Identify the three pins of the device under test. Draw the capacitance-voltage characteristics across the highly doped and least doped junctions. Extract barrier height, doping concentration,

and other parameters. Comment on it and conclude.

Measurement Condition:

a) Device under test: p-n junction Diode(IN4007)

b) Instrumental Frequency: 1Khz ,100KHz, 1MHZ

c) Modes of measurement :Cp-D, Cp-Rp, Cp-Q, Cp, OR Cs-D, Cs-Rs, Cs-Q, Cs

d) BIAS Voltage :0-5V (reverse bias)

2. Identify the components needed to build a low pass filter. Simulate the circuit using analysis

program Multisim and build the circuit on NI ELVIS II board to find the output waveform .

Comment on it and conclude.

3. Identify the device under test and draw its current-voltage Characteristics and state what electrical parametaers you can find out from the curve. Comment on it and conclude.

4.Identify the three pins of the device. Draw the current -voltage characteristics of the device and state what electrical parameters you can find out from the curve.Comment on it and conclude.

5. Surface treatment of silicon wafer by Annealing process.

6. Determination of p-type/n-type semiconductor and their charateristics using HMS3000 Hall Effect Measurement system.

7.Study on the capacitance or inductance curve of DUT by varrying the frequency up to 1MHz. Find the dissipation and the quality factor for the components. Comment on the curve to find its functionality?

Measurement Conditions: For DUT

6. Instrumental Frequency Range : 20Hz to 2MHz
7. Modes of measurement : C_p-D, C_p-R_p, C_p-Q, C_p or C_s-D, C_s-R_s, C_s-Q, C_s

Measurement Conditions: For DUT

c. Instrumental Frequency Range : 20Hz to 2MHz

d. Modes of measurement : L_p-D, L_p-R_p, L_p-Q, L_p or L_s-D, L_s-R_s, L_s-Q, L_s

9.Identify the device and its contacts. Draw the capacitance-voltage characteristics across the junction. Extract barrier height, doping concentration, and other parameters. Comment on it and conclude.

Measurement Conditions:

a) Device under test : p-n junction Diode(IN4007)

b) Instrumental Frequency : 1KHz, 100KHz, 1MHz

c) Modes of measurement : C_p-D, C_p-R_p, C_p-Q, C_p or C_s-D, C_s-R_s, C_s-Q, C_s

d) Bias Voltage : 0 to 5V (reverse bias)

PGMVD-292: VLSI Design lab II
0(L) 2(T) 2(P)

Contact hours:3P
Credit points: 2

Pre-requisites :
Student should have basic familiarity with digital design and also VLSI circuit design and should have knowledge about the Hardware Description Language (HDL).

Course Objective :
CO1- student should be familiar about VLSI Tools like DSCH, Micro-wind and Electric etc. for Schematic and Layout design.
CO2- student should be able to design digital circuit on schematic window of DSCH tool and also able to test the design.
CO3- student should be able to extract the Layout of digital circuits and CMOS circuits using Micro-wind tool.
CO1- student should be able to design CMOS circuits on schematic window of Electric and able to test it and also extract the layout.

List of Lab Assignments :
I. List of Lab assignments with DSCH and Microwind:
1. i) Learn how to install the DSCH and Microwind and familiar with DSCH Schematic .
ii) Test the basic Gates(like, AND & NAND etc.) on DSCH schematic window and Extract their layouts using Micro wind.
2. Learn to design and Test of a) Full adder using half adder and b)full subtractor using half subtractor circuit on DSCH schematic window and Extract the layout using micro wind.
3. Learn to design and Test of a) Binary adder sub tractor circuit and b) Ripple carry adder circuit on DSCH schematic window and Extract the layout using micro wind.
4. Learn to design and Test of a) Parity checker circuit and b) 2:4 decoder circuit on DSCH schematic window and Extract the layout using micro wind.
5. Learn to design and Test of a) the 4:1 mux using 2:1 mux circuit and b) 1 bit comparator circuit on DSCH schematic window and Extract the layout using micro wind.
6. Learn to design and Test of a) CMOS inverter circuit and b) CMOS- NOR circuit c) CMOS XOR circuit and d)CMOS Combinational circuit on DSCH schematic window and Extract the layout using micro wind.II. List of Lab Assignments with Electric:
1. i) Learn how to install the Electric and familiar with Schematic design and test.
ii) Test the basic Gates(like, AND & NAND etc.) on Elecric schematic window and Extract their layouts using Electric.
2. Learn to design and Test of a) full adder using half adder and b) Full subtractor circuit and Extract the layout using Electric.
3. Learn to design and Test of Ripple carry adder circuit and Extract the layout using Electric
4. Learn to design and Test of a) Binary adder subtractor circuit and b) Parity checker circuit and Extract the the layout using electric.
5. Learn to design and Test of a) 2:4 decoder circuit and b) 4:1 mux using 2:1 mux circuit and Extract the the layout using electri.c
6. Learn to design and Test of a) 1 bit comparator circuit and b) CMOS inverter and extract the the layout using electric.
7. Learn to design and Test of a) CMOS-NAND, b) CMOS-XOR and CMOS Combinational circuit and Extract the the layout using electric.

Books:
1. John P. Uyemura, Chip design for Submicron VLSI: CMOS Layout and Simulation,

Thomson, 2006.
2. Etienne S icard, User's Manual Lite Version- Microwind & Dsch Version 3.5, September 2009
3. Steven M. Rubin, Electric User's Manual, Version 9.07, 1 st Nov. 2016.

Maulana Abul Kalam Azad University of Technology, West Bengal

(Formerly West Bengal University of Technology)

Syllabus for M. Tech in Microelectronics and VLSI Technology(MVD)

(Applicable from the academic session 2019-2020)

Detailed Syllabus

Name of the course:	**ALGORITHMS**
Course Code:PGMVD301C	**Semester: 3rd**
Duration: 6 months	**Maximum Marks: 100**
Teaching Scheme	**Examination Scheme**
Theory: 3 hrs/week	Mid Semester Exam: 15 Marks
Tutorial: 1 hr/week	Assignment & Quiz: 10 Marks
Practical: 0 hrs/week	Attendance: 05 Marks
Credit Points: 4	End Semester Exam: 70 Marks

Course outcomes: At the end of the course the student should be able to:

1.	*Explain and apply graph minimization algorithms.*
2.	*Write code for algorithms used for computational and geometrical simplification and minimization using data structures for CAD tools.*
3.	*Explain and write code for partitioning, floor planning, chip planning and pin assignment.*
4.	*Explain different algorithms used for placement of cells during the physical design of a chip.*
5.	*Explain and write code for algorithms used for routing of cells, clock and power supply.*

Unit	Content	Hrs.	Marks
1	**Introduction to Algorithms:** Concept of Algorithm, The role of algorithm in computing, Fundamentals of Algorithm, Important Types of Algorithm, Fundamental Data Structures. Introduction Analysis Framework, Methodologies for Analyzing Algorithms, Amortization, and Case Studies in Algorithm Analysis. Asymptotic Notations and Basic Efficiency Classes, Mathematical Analysis of Non recursive Algorithms. Mathematical Analysis of Recursive Algorithms, empirical Analysis of Algorithms, Algorithm visualization.	10	
2	**Graph Algorithms:** Graph search Algorithms, Spanning tree Algorithm, Shortest path Algorithm, Matching Algorithm, Min cut and Max cut Algorithms and Steiner Tree Algorithm.	7	
3	**NP-Complete Problem:** NP-class of problems, P-class problems, NP=P question, Polynomial problem reduction (Reducibility), Cook's theorem, NP-hardness and NP-completeness, NP-completeness FAQ including how to handle NP-hard problems, Examples of NP-completeness proofs: SAT to 3-SAT, Polynomial-time non-deterministic algorithms, Maximum Clique Problem.	8	
4	**Computational geometry Algorithms:** Line sweep method and extended line sweep method. Basic data structures: Linked list of blocks. Graph Algorithms for physical design: Classes of graphs in physical design, relationship between graph classes, graph problems, Algorithms for interval graphs and Algorithms for permutations graphs.	5	
5	**Partitioning:** Group migration Algorithms. Floor planning and Pin assignment.	2	
6	**Placement:** Simulated annealing, simulated evolutions, force directed placement, sequence pair technique.	2	
7	**Routing:** Routing Algorithms. Shortest path algorithm, Steiner tree	6	

	based Algorithm. Single layer routing Algorithms and two layer routing Algorithms. Over the cell routing, Via minimization, clock, power and ground routing. Topological Sort.		

Suggested books

1. Naveed Sherwani, "Algorithms for VLSI Physical Design Automation" 3 rd edition, Springer international, 1998.
2. Pinaki Mazumber, Elizabeth M Rudnick, "Genetic Algorithms For VLSI Design, Layout & Test Automation", Pearson education, 2007.
3. Ellis Horowitz, sartajsahni, Sanguthevar Rajasekaran, "Fundamentals of Computer Algorithms" Universities Press.
4. Thomas H Cormen, Charles E Lieserson, Ronald L Rivest and Clifford Stein, "Introduction to Algorithms", 4TH Edition, MIT Press/McGraw-Hill.

Suggested reference books

1. Jon Kleinberg and ÉvaTardos, "Algorithm Design", 1ST Edition, Pearson.
2. Michael T Goodrich and Roberto Tamassia, "Algorithm Design: Foundations, Analysis, and Internet Examples", Second Edition, Wiley.
3. Udi Manber, Addison-Wesley, "Algorithms -- A Creative Approach", 3RD Edition, Reading, MA