# Expert Lecture Session on

## "System-on-Chip Development: Eco System, Latest Technology Trends, Design Methodology and Best Practices"

***Organized By the Department of Electrical Engineering, RCCIIT***

**Speaker: Mr. Sanjib Sarkar,** Intel Corporation, CA, USA, Principal Engineer, Analog and Mixed Signal IP Development

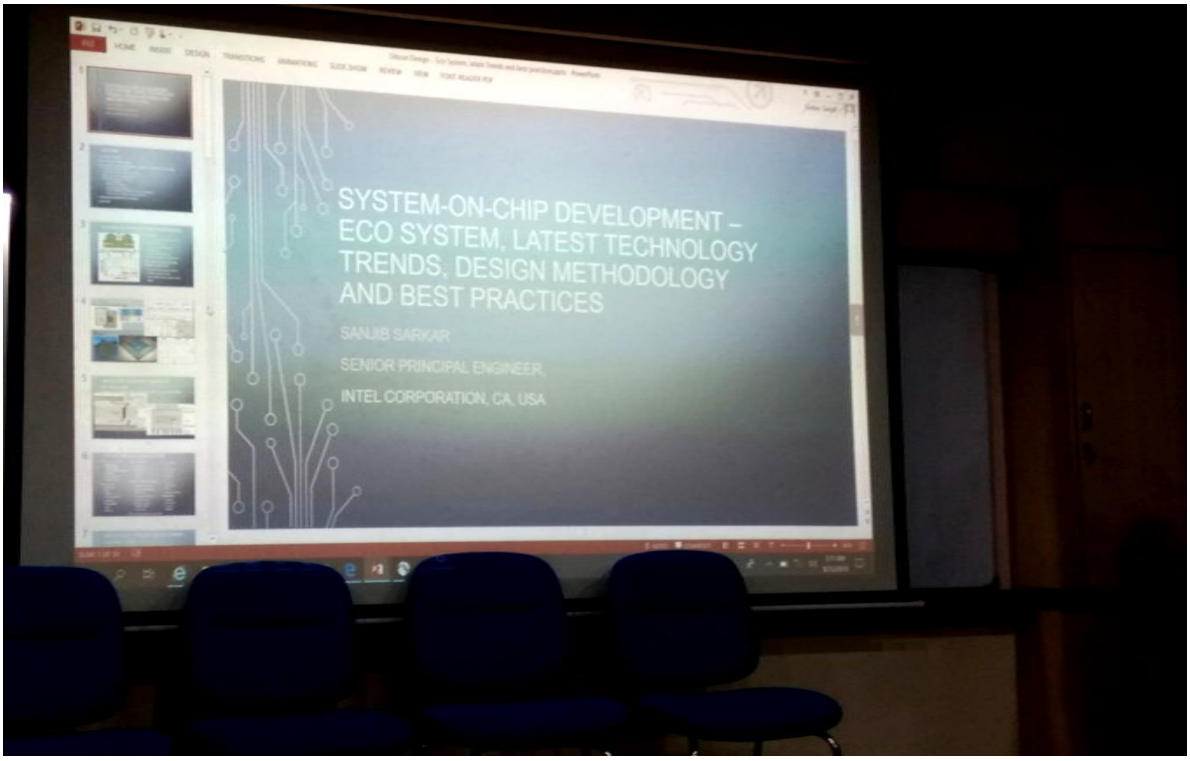
The Department of Electrical Engineering, RCCIIT has organized an expert lecture session on the topic **"System-on-Chip Development: Eco System, Latest Technology Trends, Design Methodology and Best Practices"** for Faculties, Masters, Final Year and 3rd year B.Tech students of the EE and ECE department. In view of the present technology changing scenario in VLSI processes in terms of applied science and technology, this type event was very essential for the students. The session was held on **13th, August, 2019 from 2:30-5:30 PM in Language Lab, RCCIIT old campus.** Around 50-52 participates were from the EE and ECE department has participated in the program.

Mr. Sarkar has described various steps of process in a processor (System-on-Chip or SOC) design to obtain very high speed with minimum error, lower size and low power consumption .Size is related to Economics , compactness and portability issues, Power consumption is very much important for hand held devices to have a longer time of operation with battery in between consecutive charges. Speed and reliability are the performance parameters. Mr. Sanjib Sarkar has explained how the logic of the device and IP Cores are transformed into device geometry level, and how the dimensions could be further optimized to achieve the target. He also described the process of design validation before final floor plan. He explained the effect of various circuit parameters in effecting delay and power consumption .It was very much interesting to learn how the fabrication process in the order of nano meter can take place with ultimate precision and reliability .He has also explained the expected criterion of System-on- Chip (SOC) and 3D solution of some planar architecture for better results. This lecture was targeted to Faculties and students, especially who are interested to work with VLSI processor design Industries like Intel, AMD etc. The whole session was very interesting and was really helpful for the students. It gives a deep exposure to the student for the preparation of employment in perspective of present industry requirement. It remains as a source of thinking to make a bridge between the text book knowledge and what is happening in the Industries.

Some important moments of this event are attached below this report:

*Introduction of Mr. Sanjib Sarkar by Dr. Shilpi Bhattacharya*

*Slide presentation (1) Session by Mr. Sanjib Sarkar*



*Slide presentation (2) Session by Mr. Sanjib Sarkar*


*In front of attending students and Faculty Member*

## **A Brief Bio Data of Mr. Sanjib Sarkar**:

Sanjib is a Senior Principal Engineer in the Analog and Mixed-signal-IP development division of Intel Corporation, CA, USA, specializing in high speed IO architecture and other circuit design areas. He graduated in Electrical Engineering from Jadavpur University, Calcutta, India. He obtained Master's degree in Electrical Engineering from Louisiana State University, USA. He has been working in Intel Corporation since last 24 years and played key roles in design of several major CPU's rolled out by Intel. Sanjib's design experience spans more than 8 Intel process technology nodes. Sanjib most recently led development of 20Gb/s Thunderbolt/USB/DP combo PHY and industry's first PCIE3 over TypeC USB. Earlier he led developments of first client CPU PCIe3and USB3.1 Gen2 PHYs, first 1866 DDR3/L, first 2M on-die L2 cache designs and enabled introduction of first MIM cap based power-delivery design. Sanjib has 10 patents and several others that are pending approval. He has co-authored 3 IEEE papers and several other papers that are presented in conferences internal to Intel. He has received highest Intel awards IAA and IQA along with more than 20 divisional recognition awards so far for his various contributions.