DESIGN AND DEVELOPMENT OF E-HEALTH MONITORING SYSTEM USING IOT

A Project report submitted in partial fulfillment

of the requirements for the degree of B. Tech in Electrical Engineering

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CERTIFICATE

TO WHOM IT MAY CONCERN

This is to certify that the project work entitled **DESIGN AND DEVELOPMENT OF E-HEALTH MONITORING SYSTEM USING IOT** is the bona fide work carried out by

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_____ _____

Signature of the Guide **Signature of the HOD**

Name: **Name:**

Designation: **Designation:**

_____

Signature of External Examiner

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Designation:

ACKNOWLEDGEMENT

It is our great fortune that we have got the opportunity to carry out this project work under the supervision of **Prof.(DR.)Alok Kole** in the Department of Electrical Engineering, RCC Institute of Information Technology (RCCIIT), Canal South Road, Beliaghata, Kolkata-700015, affiliated to Maulana Abul Kalam Azad University of Technology (MAKAUT), West Bengal, India. We express our sincere thanks and deepest sense of gratitude to our guide for his constant support, unparalleled guidance and limitless encouragement.

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Place: KOLKATA ----------

Date: 20/05/2020 **Full Signature of the Student**

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LIST OF ACRONYMS AND ABBREVIATIONS

1) WHO: World Health Organization
2) IoT: Internet of Things
3) CVD: Cardio Vascular Disease
4) HMS: Health Monitoring System
5) ECG: Electrocardiogram
6) GPS: Global Positioning System
7) GUI: Graphical User Interface
8) WSN: Wireless Sensor Network
9) SMS: Short Message Service
10) Wi-Fi: Wireless Fidelity
11) MCU: Micro Controller Unit
12) TCP: Transmission Control Protocol
13) IP: Internet Protocol
14) IDE: Integrated Development Environment
15) VCC: Voltage Common Collector
16) ADC: Analog to Digital Converter
17) IR: Infrared
18) LED: Light Emitting Diode
19) BPM: Beats per minute
20) ODE: Ordinary Differential Equation

LIST OF FIGURES

ABSTRACT

As per WHO statistics, cardiovascular diseases (CVDs) are the number 1 cause of death globally, taking an estimated 17.9 million lives each year (31% of all deaths worldwide). Four out of 5CVD deaths are due to heart attacks and strokes, and one third of these deaths occur prematurely in people under 70 years of age.

Health conditions of aged people usually need to be checked more frequently, which poses a greater challenge to existing medical systems. Therefore, how to identify human diseases in a timely and accurate manner with low costs has been paid an increasing attention.

Smart and cost effective healthcare has been in increasing demand to meet the needs of growing human population and medical expenses. There is an urgent need to develop an effective health monitoring system that can detect abnormalities of health conditions in time and make diagnosis according to the obtained data. Recent advances in mobile technology and cloud computing have inspired numerous designs of cloud-based health care services and devices. Within the cloud system, medical data can be collected and transmitted automatically to medical professionals from anywhere and feedback can be returned to patients through the network. In this project, we have designed and developed an E-Health Monitoring System (HMS) using an IoT platform.

INTRODUCTION

With fast paced technological advancement in the recent years, wireless technology has had a huge impact in various sectors. Internet of Things (IoT) has managed to take over most of industrial area specially automation and control, including the field of health and biomedicine. Not only in hospitals but also the personal health caring facilities are governed by the IoT technology. In traditional method, doctors play an important role in health check-up. This process requires a lot of time for registration, appointment and then check-up. Also reports are generated later. Due to this lengthy process, working people tend to ignore the check-ups or postpone it. As a solution to this, remote monitoring enables medical professionals to monitor a patient remotely using various technological devices. These services can provide comparable health outcomes to traditional in-person patient encounters, supply greater satisfaction to patients, and can also prove to be cost-effective.

With increasing popularity of mobile internet and usage of Wireless Sensor Networks (WSNs) it is now possible to have wearable/portable health monitoring systems which can monitor and record long term health parameters cost effectively without the need to visit any hospitals or diagnostic centers frequently. The two driving factors of this technology are the IoT-based data collection and cloud-based analytics.

In this project, a prototype has been designed and developed for real time health monitoring using Internet of Things (IoT). This system facilitates the process of performing diagnosis and treatment of patients suffering from heart diseases. Non-intrusive sensors DS18B20, MAX30100, and AD8232 are used for recording patient's health parameters like body temperature, heart rate, and ECG signals respectively. The data gathered is transmitted to the IoT cloud which can be visualized using a web based server or any android based application. Using this system the physician can use the cloud platform to diagnose patients at remote locations (like home). The patients can also access their medical records via this cloud service. These data can be analyzed by a doctor at remote location or can be saved and retrieved later for analysis.

OBJECTIVES AND AIM OF THE PROJECT

In order to overcome the aforesaid problems in health monitoring, the goal of this project has been to implement an IOT based E-health monitoring system which monitors the patient's body parameters such as body temperature, pulse rate, oxygen level in blood and ECG of the heart regularly, and also send the data over the internet which will be retrieved by the doctors for diagnosis and close family members, receiving regular updates as well.

Thus, the patients will be able to manage the task of taking care of their health simultaneously along with their busy life schedule.

The system is also cost-effective, portable, and easy to operate with no complex circuitry involved which adds to its advantages, being highly user friendly for the common and elderly people.

LITERATURE SURVEY

The project prototype has been developed after a systematic survey on the reviews of some previous work in the wireless sensor network area and the use Internet of Things in cardiac health monitoring.

- Many applications are now-a-days available where use of smart phones in health monitoring is experimented. Such system consisted of a wearable device comprising of Temperature and Pulse sensors. The device will send its data to the server through the android application. This data will be available to the doctor using his android application. [1]
- While few authors presented the development of a microcontroller based system for wireless heartbeat and temperature monitoring using ZigBee. The system is developed for home use by patients that are not in a critical condition but need to be constant or periodically monitored by clinician or family. In any critical condition the SMS is send to the doctor or any family member. So that we can easily save many lives by providing them quick service. [2],[4]
- Some of the authors proposed a remote mobile health monitoring system with mobile phone and web service capabilities. It provides doctors and family members with necessary data through a web interface and enables authorized personnel to monitor the patient's condition and to facilitate remote diagnosis. [3]
- In some papers, the authors have proposed an initial prototype development for wireless transmission of ECG signals using AD8232 sensor and raspberry pi based on IoT. [5]
- In some papers, a Smartphone based remote health monitoring system using body temperature and heart beat sensors to continuously monitor body parameters of cardiac patients, has been proposed using GPS to track location and wireless communication. The link is established between the patient's Bluetooth enabled Mobile device and sensors via a Bluetooth modem, this helps in continuous monitoring. [6]

- An IoT-based ECG monitoring system was developed consisting of three main parts, i.e., the ECG sensing network, IoT cloud, and GUI. Through a wearable monitoring node with three electrodes, real-time ECG signals can be collected with satisfactory accuracy. The gathered data were transmitted to the IoT cloud using Wi-Fi, which supports high data rates and wide coverage areas. [7],[8]
- A paper developed a portable, low cost ECG data acquisition system with overall less complex circuitry. Results were presented using MATLAB and Raspberry Pi.[9]

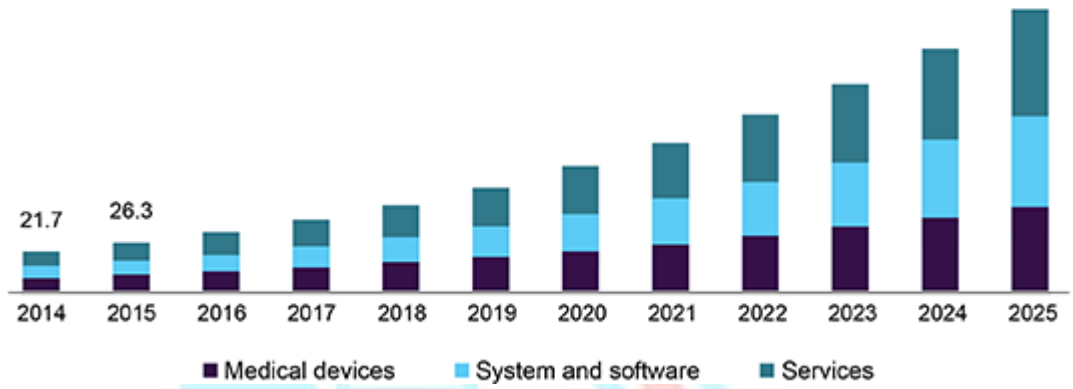


Fig.1: Projection of IoT in worldwide healthcare market size, by component, 2014-2025 (USD Billion)

THEORY

WORKING PRINCIPLE:

This project works on the main principles of IoT and sending acquired data over Cloud. All the wearable sensors used to measure the body parameters of the patient are centrally connected to a NodeMCU (ESP8266) which collects the data and sends the same over cloud and displays the respective outputs remotely on an application. The data is transferred using TCP/IP communications securely.

- ***Internet of Things (IoT)-*** Internet of Things (IoT) is an ecosystem of connected physical objects that are accessible through the internet. The 'thing' in IoT could be a person with a heart monitor or an automobile with built-in-sensors, i.e. objects that have been assigned an IP address and have the ability to collect and transfer data over a network without manual assistance or intervention. The embedded technology in the objects helps them to interact with internal states or the external environment, which in turn affects the decisions taken. It enables devices/objects to observe, identify and understand a situation or the surroundings without being dependent on human help. It can connect devices embedded in various systems to the internet. When devices/objects can represent themselves digitally, they can be controlled from anywhere. The connectivity then helps us capture more data from more places, ensuring more ways of increasing efficiency and improving safety and IoT security. IoT is basically categorized into 6 major layers. They are:
  a) Smart devices and Controllers
  b) Connectivity and protocol Communication
  c) Cloud Server
  d) Data Storage and Accumulation
  e) Data analysis and Computing
  f) User Application and Report Generation

- ***Cloud-*** Cloud computing is a general term for anything that involves delivering hosted services over the internet. These services are divided into three main categories: infrastructure as a service (IaaS), platform as a service (PaaS) and software as a service (SaaS). A cloud can be private or public. A public cloud sells services to anyone on the internet. A private cloud is a proprietary network or a data center that supplies hosted services to a limited number of people, with certain access and permissions settings. Cloud service can be used for uploading and storing of data which can be accessed from anywhere using some specific web user end servers or applications.

  IoT cloud refers to any number of cloud services that power the IoT. These include the underlying infrastructure needed for processing and storing IoT data, whether in real time or not. IoT cloud also includes the services and standards necessary for connecting, managing, and securing different IoT devices and applications. As with other types of cloud services, such as software-as-a-service, organizations consume IoT cloud services as they need them, rather than building a data center or other on-premises infrastructure to deliver those services locally.

- ***Remote Health Monitoring System-*** Remote health monitoring is growing in popularity as both patients and healthcare professionals want health to be monitored outside of clinical settings. Remote health monitoring, also referred to as remote patient monitoring, is the process of using technology to monitor patients in non-clinical environments, such as in the home. When incorporated in the management of chronic diseases, remote health monitoring has the potential to significantly improve quality of life for patients and so it should come as no surprise that this technology is growing increasingly popular. Remote health monitoring is a diverse field but the associated technologies normally share some similar components. Firstly, a monitoring device requires a sensor which can measure specific physiological data and wirelessly communicate this information to both the patient and healthcare professionals. This system enables medical check-ups and health care to be provided remotely as well as decreases health care delivery costs.

- ***IoT Platform (Blynk)-*** In our project, we have used Blynk as our IoT platform. It is specifically designed for the development and implementation of smart IoT devises quick and easily. Blynk is a Platform with IOS and Android apps to control Arduino, Raspberry Pi and similar microcontroller boards over the Internet. It's a digital dashboard where we can build a graphic interface for our project by simply dragging and dropping widgets. Blynk supports the connection types like Wi-Fi, Ethernet, Bluetooth, Cellular, Serial to connect our microcontroller board (hardware) with the Blynk Cloud and Blynk's personal server. The Blynk platform includes the following components:

  Blynk app builder: Allows building apps for our projects using various widgets. It is available for Android and iOS platforms.
  Blynk server: Responsible for all the communications between our mobile device that's running the Blynk app and the hardware. We can use the Blynk Cloud or run our private Blynk server locally. Its open source, could easily handle thousands of devices, and can even be launched on a Raspberry Pi.
  Blynk libraries: Enables communication with the server and processes all the incoming and out coming commands from our Blynk app and the hardware. They are available for all the popular hardware platforms.
  All the aforementioned components communicate with each other to build a fully functional IoT application that can be controlled from anywhere through a preconfigured connectivity type. We can control our hardware from the Blynk app running on our mobile device through the Blynk Cloud or Blynk's personal server. It works the same in the opposite direction by sending rows of processed data from hardware to our Blynk app.

- ***Electrocardiogram (ECG)-*** An ECG is simply a representation of the electrical activity of the heart muscle as it changes with time, usually printed on paper for easier analysis. Like other muscles, cardiac muscle contracts in response to electrical *depolarization* of the muscle cells. It is the sum of this electrical activity, when amplified and recorded for just a few seconds that we know as an ECG. The normal cardiac cycle begins with spontaneous depolarization of the sinus node, an area of specialized tissue situated in the high right atrium (RA). A wave of

electrical depolarization then spreads through the RA and across the inter-atrial septum into the left atrium (LA). The atria are separated from the ventricles by an electrically inert fibrous ring, so that in the normal heart the only route of transmission of electrical depolarization from atria to ventricles is through the atrioventricular (AV) node. The AV node delays the electrical signal for a short time, and then the wave of depolarization spreads down the interventricular septum (IVS), via the bundle of His and the right and left bundle branches, into the right (RV) and left (LV) ventricles. Hence with normal conduction the two ventricles contract simultaneously, this is important in maximising cardiac efficiency. After complete depolarization of the heart, the myocardium must then *repolarise*, before it can be ready to depolarize again for the next cardiac cycle. The ECG is measured by placing a series of electrodes on the patient's skin
– so it is known as the 'surface' ECG.

The wave of electrical depolarization spreads from the atria down though the IVS to the ventricles. So the direction of this depolarization is usually from the superior to the inferior aspect of the heart. The direction of the wave of depolarization is normally towards the left due to the leftward orientation of the heart in the chest and the greater muscle mass of the left ventricle than the right. This overall direction of travel of the electrical depolarization through the heart is known as the *electrical axis*.

A fundamental principle of ECG recording is that when the wave of depolarization travels toward a recording lead these results in a positive or upward deflection. When it travels away from a recording lead this results in a negative or downward deflection. The electrical axis is normally downward and to the left but we can estimate it more accurately in individual patients if we understand from which 'direction' each recording lead measures the ECG.

An essential feature of the ECG is that the electrical activity of the heart is shown as it varies with time. In other words we can think of the ECG as a graph, plotting electrical activity on the vertical axis against time on the horizontal axis. Standard ECG paper moves at 25 mm per second during real-time recording. This means that when looking at the printed ECG a distance of 25 mm along the horizontal axis represents 1 second in time.

ECG paper is marked with a grid of small and large squares. Each small square represents 40 milliseconds (ms) in time along the horizontal axis and each larger square contains 5 small squares, thus representing 200 ms. Standard paper speeds and square markings allow easy measurement of cardiac timing intervals. This enables calculation of heart rates and identification of abnormal electrical conduction within the heart.

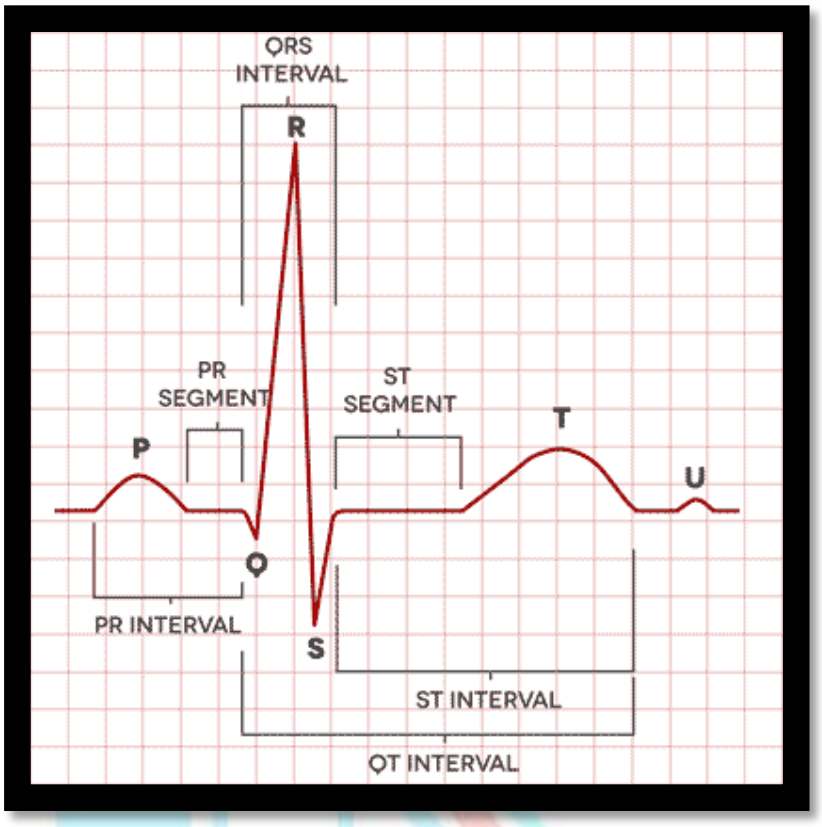


Fig.2: ECG wave analysis

- P-waves represent atrial depolarization.
- PR interval- It represents the time taken for electrical activity to move between the atria and ventricles.
- QRS complex- The QRS-complex represents depolarization of the ventricles.
- ST segment- The ST segment is an isoelectric line that represents the time between depolarization and repolarization of the ventricles (i.e. contraction).
- T-wave -The T-wave represents ventricular repolarization.
- QT-interval- It represents the time taken for the ventricles to depolarize and then repolarise.

COMPONENTS USED

Hardware Requirements:-

- ✓ NodeMCU – ESP8266
- ✓ Temperature sensor – DS18B20
- ✓ Heart rate and SPO2 sensor- MAX30100
- ✓ ECG sensor- AD8232 sensor
- ✓ Three lead electrodes
- ✓ Breadboard
- ✓ Jumper wires
- ✓ Power source

Software Requirements:-

- ✓ Arduino IDE
- ✓ FRITZING
- ✓ BLYNK

BLOCK DIAGRAM

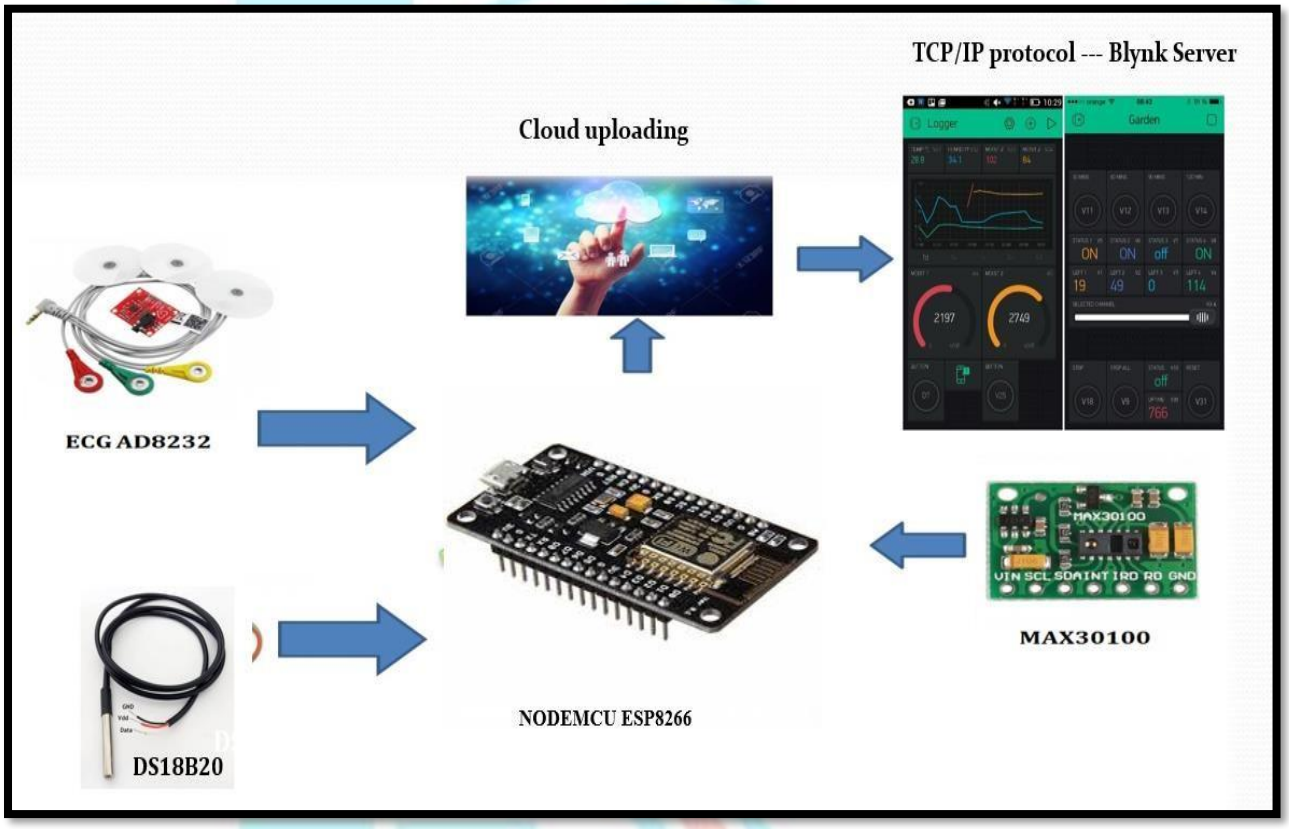


Fig.3: Block diagram showing the different interconnected parts of the model

CIRCUIT DIAGRAM

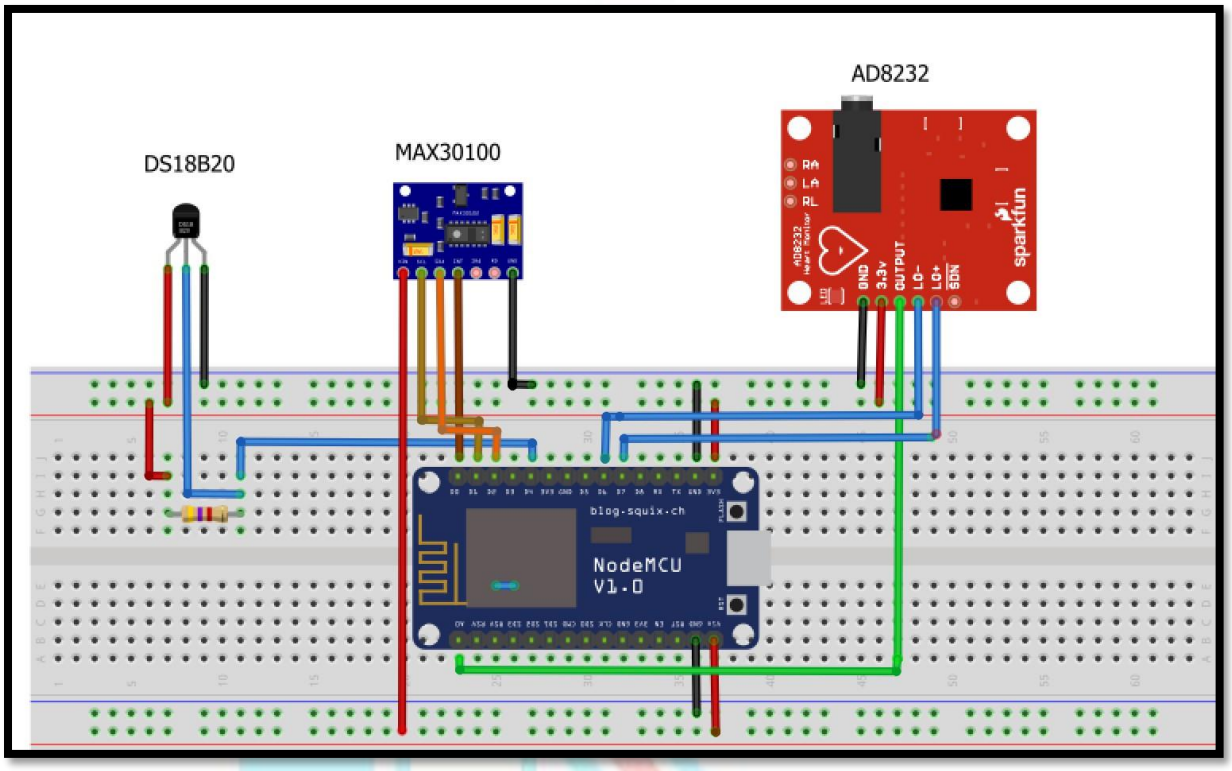


Fig.4: Overall Connection Diagram of Interfacing of DS18B20,MAX30100, AD8232 with NodeMCU

Working Principle of various sensors used:-

1) *Temperature Sensor DS18B20 –*

- This sensor basically works on the one wire communication protocol which places a resistor in between the VCC and the signal pin of DS18B20 to make it by default in the high state.
- This is a digital sensor with 12-bit of ADC embedded.
- The usable temperature range is from -55 to 125 degree Celsius as well as it has a temperature limit alarm system.

2) *Pulse Oximeter MAX30100-*

- This sensor works on the protocol of I2C communication which enables the SCL and SDA pin of the sensor to communicate with the microcontroller.
- This sensor particularly has two mode- infrared and red LEDs.
- So whenever we are trying to inhale the oxygen which subsequently increases the oxygenated blood into our body results in the absorption of the more infrared signal than that of red lights so in common terminology the SPO2 increases.
- And vice versa when we exhale, the deoxygenated blood is more than that of oxygenated blood which particularly absorbs more of the red lights and pass the infrared lights .
- And in course of time the interval in between the two basic functioning which are oxygenated and deoxygenated blood results in calculating of the heart rate in BPM .

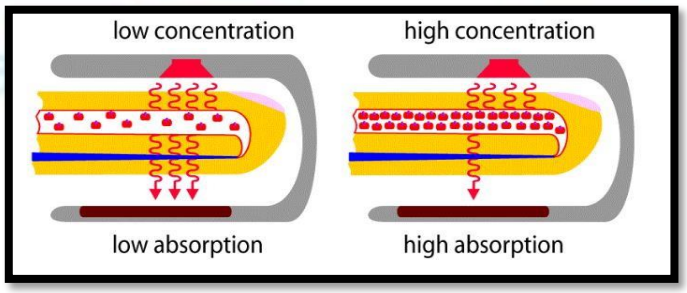


Fig.5: Working of MAX30100

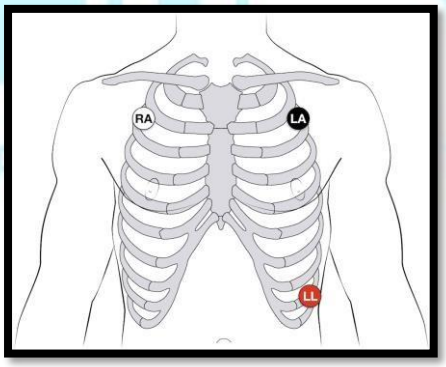
3) <u>ECG Sensor Module AD8232-</u>

- Whenever the body is connected with the electrodes of the ECG sensor, it conducts electrical signals from the skin surface with the help of gel present in the electrodes.
- With every oxygenated and deoxygenated blood pumps in and out, there happens to be an electrical energy spreading around the body but that is of very low power which in turn is not felt by us.
- In this case the conductive gel present inside the electrodes conducts that low power electrical signal and finally amplifies the signal in order to get the analog values of the ECG which is later on plotted on the ECG paper.

Fig.6a & 6b: Lead Electrodes and conducting gel

3 lead Placement (I, II, or III):

- RA: electrode: Placed under right clavicle near right shoulder, within the rib cage frame.
- LA: electrode: Placed under left clavicle, near left shoulder, within the rib cage frame.
- LL: electrode: Placed on the left side, below pectoral muscles, lower edge of left rib cage.



MATHEMATICAL MODEL

As the ECG is a vital aspect of our project, a study of the numerical simulation and mathematical model of electro cardio-grams (ECG) was deemed necessary.

The main ingredients of this model are classical: the bidomain equations coupled to a phenomenological ionic model in the heart, and a generalized Laplace equation in the torso.

This macroscopic model is based on the assumption that, at the cell scale, the cardiac tissue can be viewed as partitioned into two ohmic conducting media, separated by the cell membrane: intracellular, made of the cardiac cells, and extracellular which represents the space between them. After an homogenization process, the intra- and extracellular domains can be supposed to occupy the whole heart volume Ω_H (this also applies to the cell membrane). Hence, the averaged intra- and extracellular densities of current, j_i and j_e, conductivity tensors, σ_i and σ_e, and electric potentials, u_i and u_e, are defined in Ω_H. The electrical charge conservation becomes

$$\operatorname{div}(j_i + j_e) = 0, \quad \text{in} \quad \Omega_H \tag{1.1}$$

and the homogenized equation of the electrical activity of the cell membrane is given by

$$A_m \left(C_m \frac{\partial V_m}{\partial t} + I_{ion}(V_m, w) \right) + \operatorname{div}(j_i) = A_m I_{app}, \quad \text{in} \quad \Omega_H, \tag{1.2}$$

complemented with the Ohm's laws

$$j_i = -\sigma_i \nabla u_i, \quad j_e = -\sigma_e \nabla u_e \tag{1.3}$$

Here, V_m stands for the transmembrane potential, defined as

$$V_m \stackrel{\text{def}}{=} u_i - u_e, \tag{1.4}$$

A_m is a constant representing the rate of membrane area per volume unit and C_m the membrane capacitance per area unit. The term $I_{ion}(V_m, w)$ represents the ionic current across the membrane and I_{app} a given applied current stimulus. Both currents are measured per membrane area unit.

In general, the ionic variable w (possibly vector valued) satisfies a system of ODE of the type:

$$\frac{\partial w}{\partial t} + g(V_{\mathrm{m}}, w) = 0, \quad \text{in} \quad \Omega_{\mathrm{H}}. \tag{1.5}$$

The functions g and I_{ion} are then given by

$$I_{\mathrm{ion}}(V_{\mathrm{m}}, w) = -\frac{w}{\tau_{\mathrm{in}}} \frac{(V_{\mathrm{m}} - V_{\mathrm{min}})^2 (V_{\mathrm{max}} - V_{\mathrm{m}})}{V_{\mathrm{max}} - V_{\mathrm{min}}} + \frac{1}{\tau_{\mathrm{out}}} \frac{V_{\mathrm{m}} - V_{\mathrm{min}}}{V_{\mathrm{max}} - V_{\mathrm{min}}},$$

$$g(V_{\mathrm{m}}, w) = \begin{cases} \dfrac{w}{\tau_{\mathrm{open}}} - \dfrac{1}{\tau_{\mathrm{open}}(V_{\mathrm{max}} - V_{\mathrm{min}})^2} & \text{if} \quad V_{\mathrm{m}} < V_{\mathrm{gate}}, \\ \dfrac{w}{\tau_{\mathrm{close}}} & \text{if} \quad V_{\mathrm{m}} > V_{\mathrm{gate}}, \end{cases} \tag{1.6}$$

where τ_{in}, τ_{out}, τ_{open}, τ_{close}, V_{gate} are given parameters and V_{min}, V_{max} scaling constants (typically -80 and 20 mV, respectively).

The gate variable w depends on the change-over voltage V_{gate} and on the time constants for opening, τ_{open}, and closing, τ_{close}. The time constants τ_{in} and τ_{close} are respectively related to the length of the depolarization and repolarization (final stage) phases. Typically, these constants are such that $\tau_{\mathrm{in}} \ll \tau_{\mathrm{out}} \ll \tau_{\mathrm{open}}, \tau_{\mathrm{close}}$. To sum up, the system of equations modeling the electrical activity within the heart is

$$\begin{cases} A_{\mathrm{m}} \left(C_{\mathrm{m}} \dfrac{\partial V_{\mathrm{m}}}{\partial t} + I_{\mathrm{ion}}(V_{\mathrm{m}}, w) \right) - \mathrm{div}(\boldsymbol{\sigma}_{\mathrm{i}} \boldsymbol{\nabla} V_{\mathrm{m}}) - \mathrm{div}(\boldsymbol{\sigma}_{\mathrm{i}} \boldsymbol{\nabla} u_{\mathrm{e}}) = A_{\mathrm{m}} I_{\mathrm{app}}, & \text{in} \quad \Omega_{\mathrm{H}}, \\ -\mathrm{div}((\boldsymbol{\sigma}_{\mathrm{i}} + \boldsymbol{\sigma}_{\mathrm{e}}) \boldsymbol{\nabla} u_{\mathrm{e}}) - \mathrm{div}(\boldsymbol{\sigma}_{\mathrm{i}} \boldsymbol{\nabla} V_{\mathrm{m}}) = 0, & \text{in} \quad \Omega_{\mathrm{H}}, \\ \dfrac{\partial w}{\partial t} + g(V_{\mathrm{m}}, w) = 0, & \text{in} \quad \Omega_{\mathrm{H}}, \end{cases} \tag{1.7}$$

with g and I_{ion} given by (1.6). This system has to be complemented with appropriate initial and boundary conditions. Denoting by V_m^0 and w^0 given initial data for the transmembrane potential and the gate variable, the following initial condition must be enforced

$$V_{\mathrm{m}}(\mathbf{x}, 0) = V^0(\mathbf{x}), \quad w(\mathbf{x}, 0) = w^0(\mathbf{x}) \quad \forall \mathbf{x} \in \Omega_{\mathrm{H}} \tag{1.8}$$

As regards the boundary conditions on $\Sigma \stackrel{\mathrm{def}}{=} \partial\Omega$ (see Figure 1), it is widely assumed that the intracellular current does not propagate outside the heart. Consequently,

$$j_i \cdot n = \sigma_i \nabla u_i \cdot n = 0, \text{ on } \Sigma$$

where n stands for the outward unit normal to ΩH. Equivalently, and owing to the divergence structure of (1.7), this condition can be

enforced as

$$\sigma_i \nabla V_m \cdot n + \sigma_i \nabla u_e \cdot n = 0, \text{ on } \Sigma. \qquad (2.9)$$

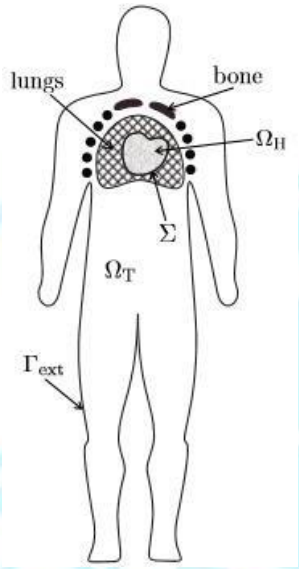


Fig.8: Geometry description: the heart domain ΩH and the torso domain ΩT (extra myocardial regions)

INDIVIDUAL CONNECTION DIAGRAMS: –

1)

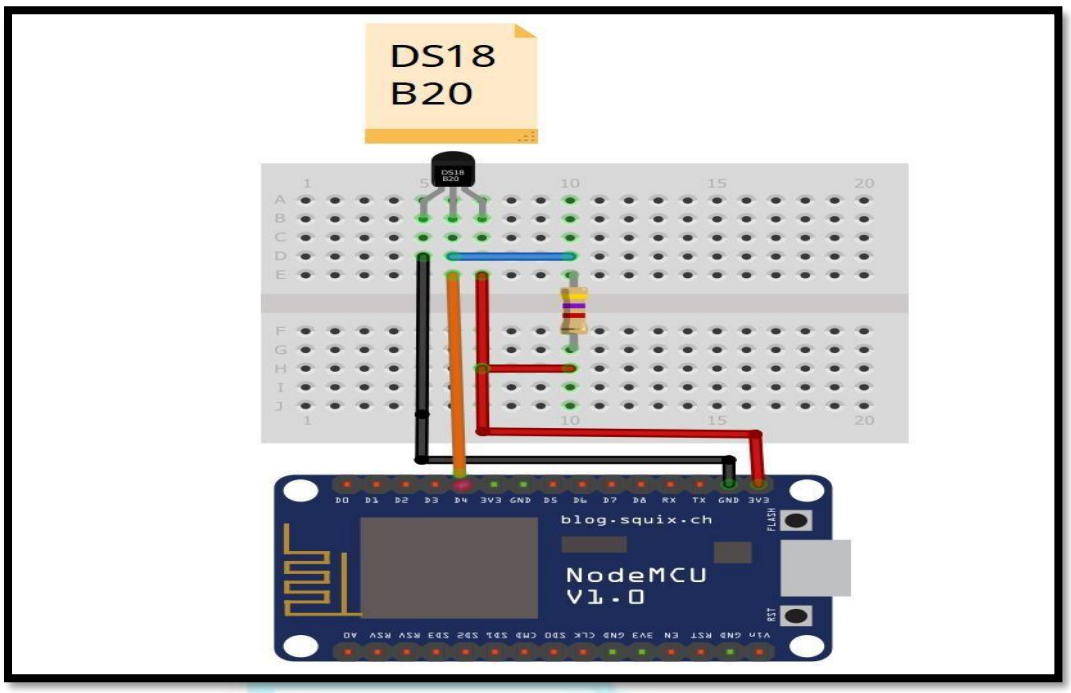


Fig9: Interfacing DS18B20 with NodeMCU

- NodeMCU 3.3V ------ -- 3.3V pin
- NodeMCU Digital Pin ------ D4
- NodeMCU Gnd ---------- Gnd
- A pull up resistor of 4.7K in between the VCC and Signal pin.

2)

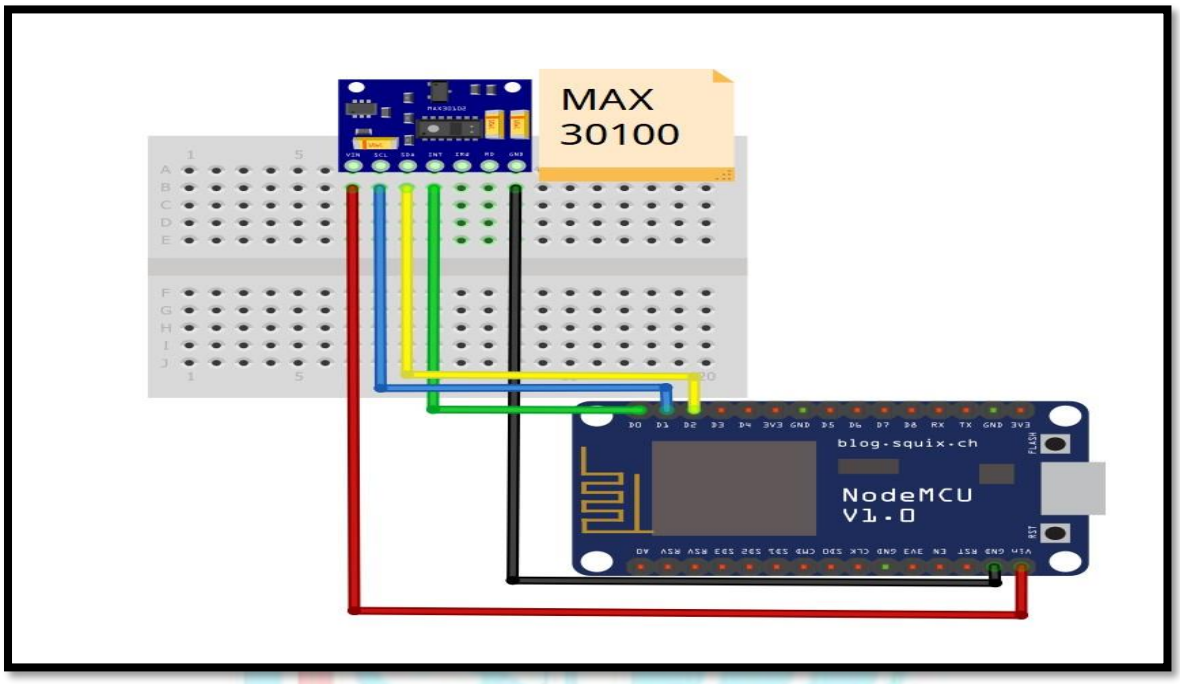


Fig.10: Interfacing MAX30100 with NodeMCU

- NodeMCU Vin---------- n of MAX30100
- NodeMCU pin D1-------- SCL
- NodeMCU Pin D2-------- SDA
- NodeMCU Pin D0-------- INT
- NodeMCU Analog (A0) ----- Output
- NodeMCU Gnd---------- Gnd

3)

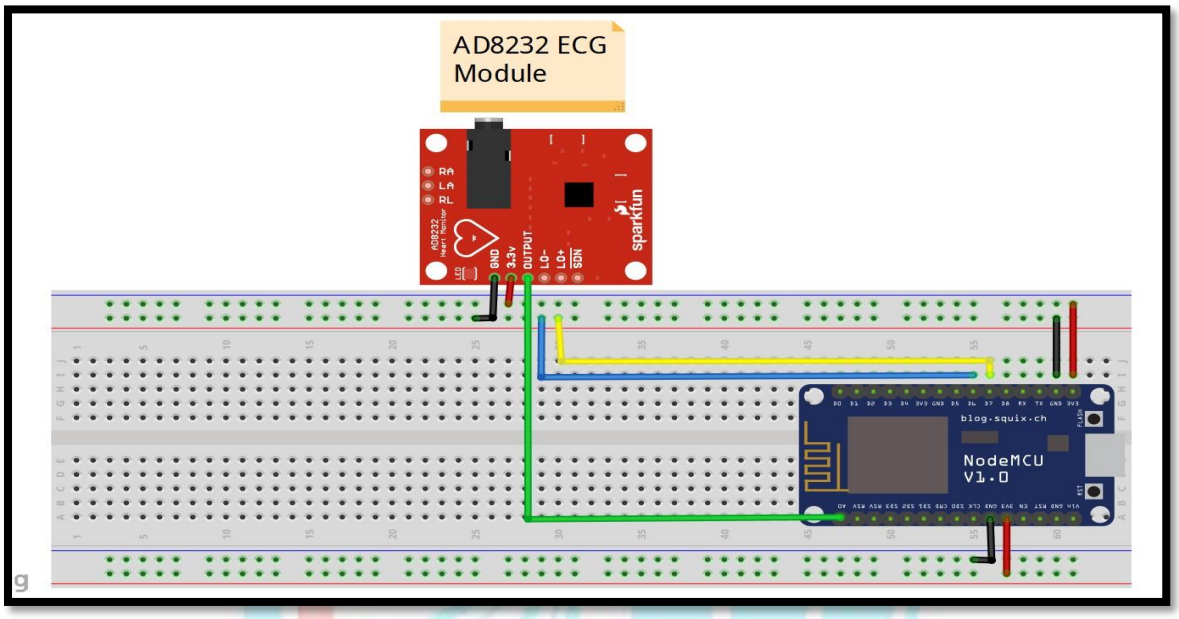


Fig.11: Interfacing AD8232 with NodeMCU

- NodeMCU 3.3V ------ -- 3.3V pin
- NodeMCU pin D7---------L0+
- NodeMCU Pin D6---------L0-
- NodeMCU Analog (A0)-----Output
- NodeMCU Gnd---------- Gnd

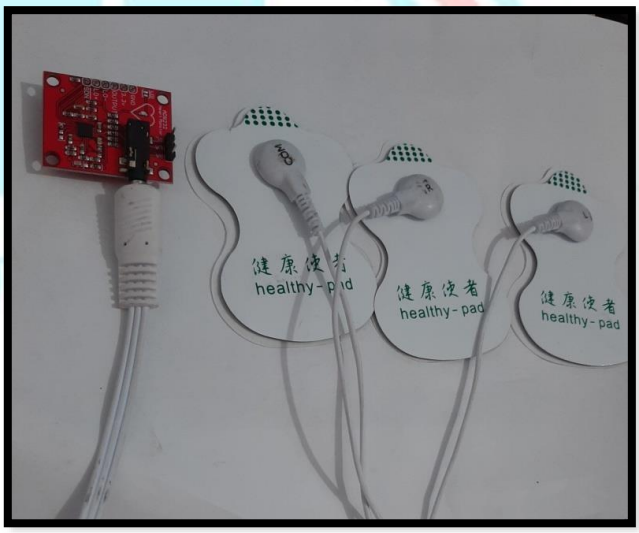


Fig.12: AD8232 Module

HARDWARE MODEL

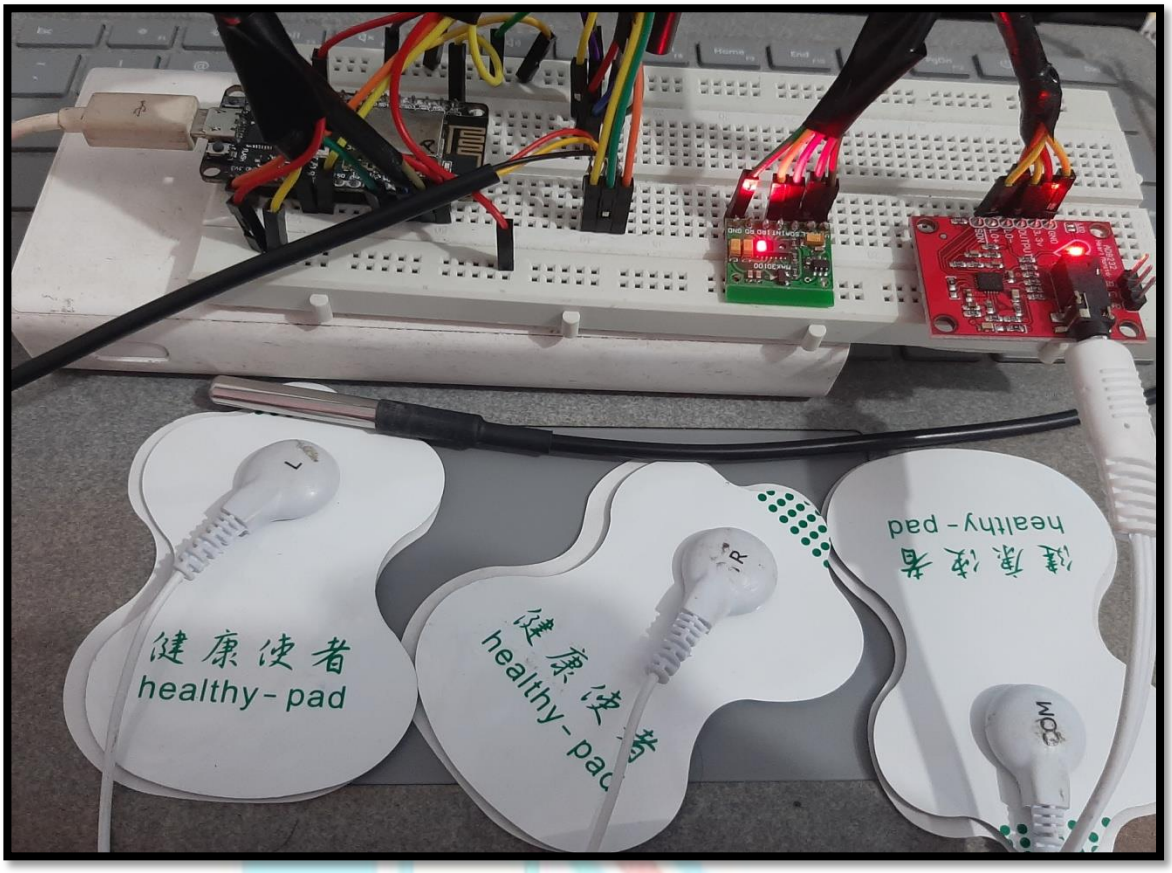
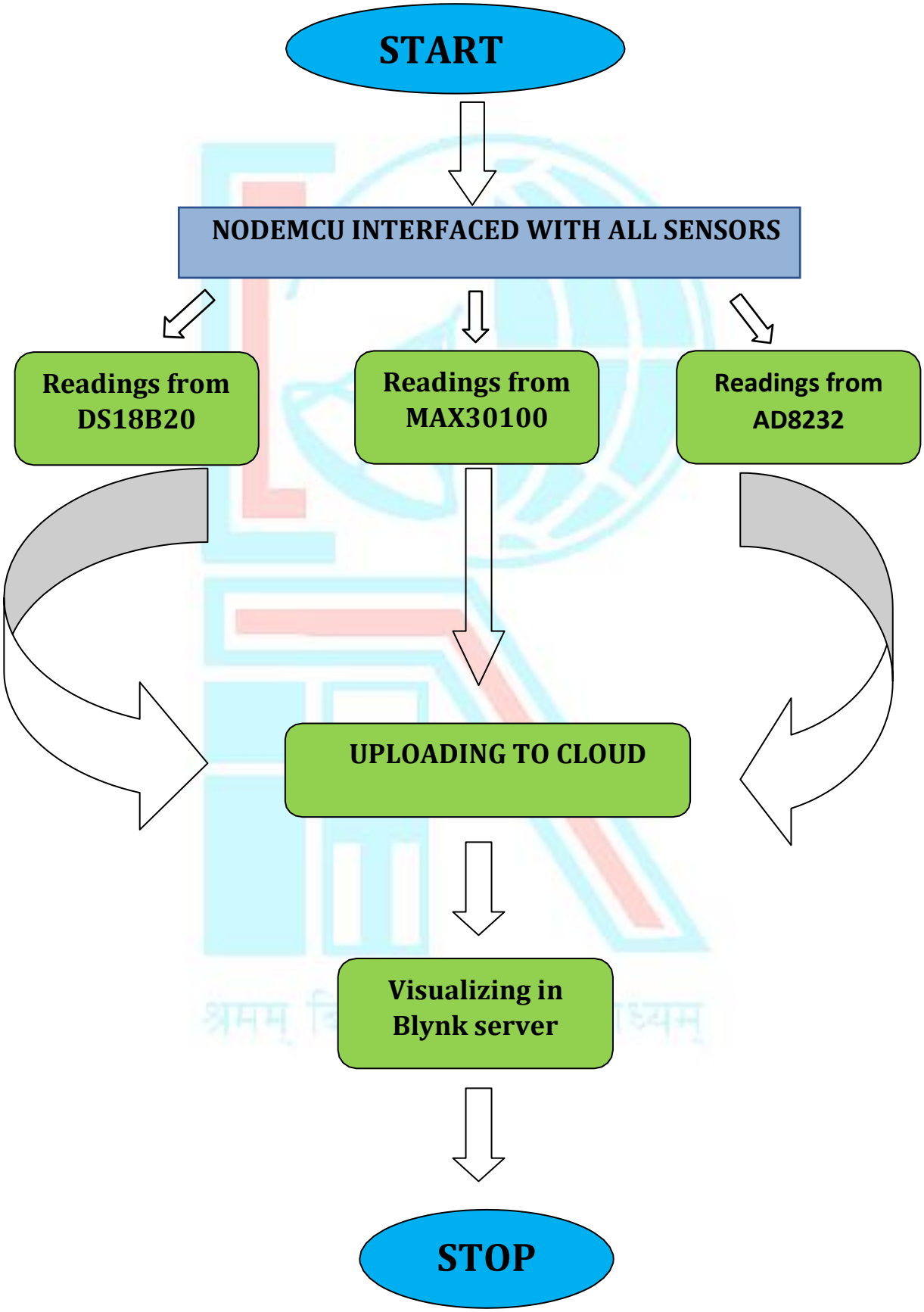


Fig.13: Physical connection layout of hardware model

FLOW CHART


START
NODEMCU INTERFACED WITH ALL SENSORS
Readings from DS18B20
Readings from MAX30100
Readings from AD8232
UPLOADING TO CLOUD
Visualizing in Blynk server
STOP

SOFTWARE PROGRAM

- **SOURCE CODE FOR DS18B20 WITH NodeMCU-**

```
#include <BlynkSimpleEsp8266.h>
#include <SimpleTimer.h>
#include <OneWire.h>
#include <DallasTemperature.h>
#include <ESP8266WiFi.h>
#define BLYNK_PRINT Serial
char auth[] = "wTY9Evzq9JyHHs1HT3EduxuWtznD****";

/* WiFi credentials */
char ssid[] = "D-Link_PRASUN";
char pass[] = "12345";

SimpleTimer timer;
#define ONE_WIRE_BUS 2
DallasTemperature DS18B20(&oneWire);
float temp;
float Fahrenheit=0;

void setup()
```

```
{
  Serial.begin(115200);
  Blynk.begin(auth, ssid, pass);
  DS18B20.begin();

  timer.setInterval(1000L, getSendData);
void loop()
{
  timer.run(); // Initiates SimpleTimer
  Blynk.run();
}
void getSendData()
{
  DS18B20.requestTemperatures();
  Serial.print("Celsius= ") ;
  temp = DS18B20.getTempCByIndex(0); // Celcius
  Fahrenheit = DS18B20.toFahrenheit(temp); // Fahrenheit
  Serial.println(temp);
  //Serial.println(Fahrenheit);
  Blynk.virtualWrite(V3, temp);
}
```

Output-

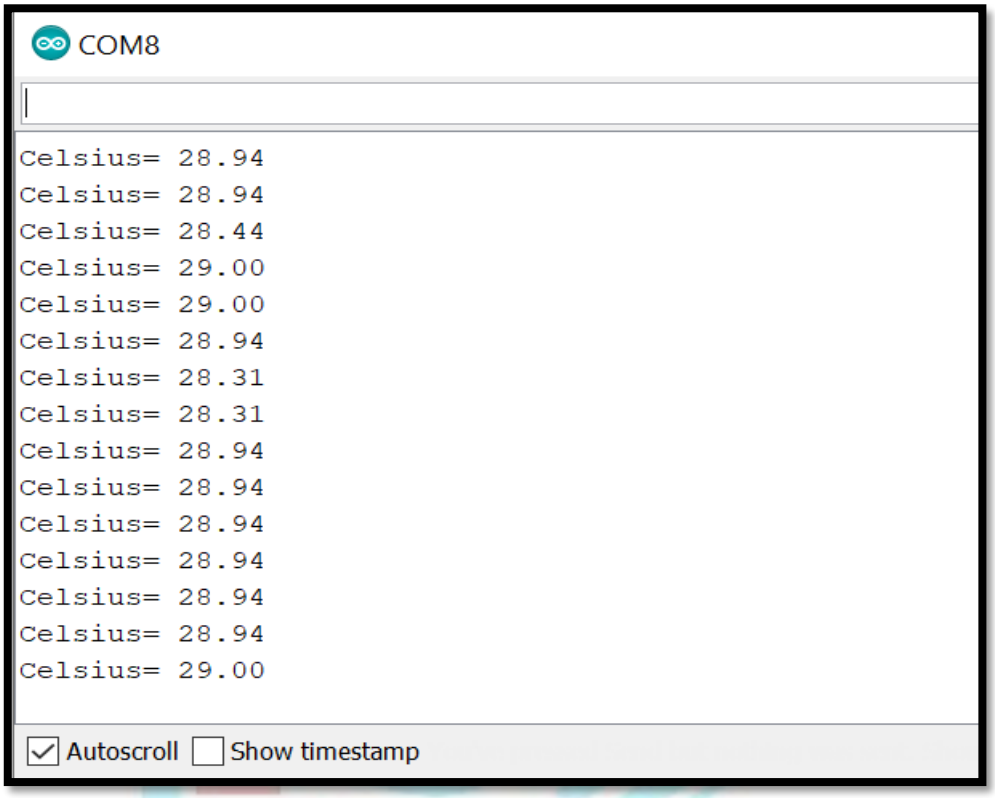


Fig. 24:Output of Temperature Sensor as shown in serial monitor

➢ SOURCE CODE FOR MAX30100 WITH NODEMCU

```
#include <BlynkSimpleEsp8266.h>

#include "MAX30100_PulseOximeter.h"

#include <ESP8266WiFi.h>

#include <Wire.h>

#define BLYNK_PRINT Serial

char auth[] = "wTY9Evzq9JyHHs1HT3EduxuWtznD****";

/* WiFi credentials */

char ssid[] = "D-Link_PRASUN";
```

```
char pass[] = "12345”;


PulseOximeter pox;

float BPM, SpO2;

uint32_t tsLastReport = 0;

#define REPORTING_PERIOD_MS 1000

void onBeatDetected()

{

   Serial.println("Beat Detected!");

}

void setup()

{

 Serial.begin(115200);

 Blynk.begin(auth, ssid, pass);

 DS18B20.begin();

  Serial.print("Initializing Pulse Oximeter..");

if (!pox.begin())

   {

       Serial.println("FAILED");

 }

   else

   {

       Serial.println("SUCCESS");
```

```
    }
    pox.setIRLedCurrent(MAX30100_LED_CURR_7_6MA);
    pox.setOnBeatDetectedCallback(onBeatDetected);
}

void loop()
{
  Blynk.run();
  pox.update();
  if (millis() - tsLastReport > REPORTING_PERIOD_MS)
    {
          BPM = pox.getHeartRate();
        SpO2 = pox.getSpO2();
        Serial.print("Heart rate:");
        Serial.print(BPM);
        Serial.print(" bpm / SpO2:");
        Serial.print(SpO2);
        Serial.println(" %");

        Blynk.virtualWrite(V7,  BPM);
        Blynk.virtualWrite(V8, SpO2);
        tsLastReport = millis();
    }
}
```

Output-

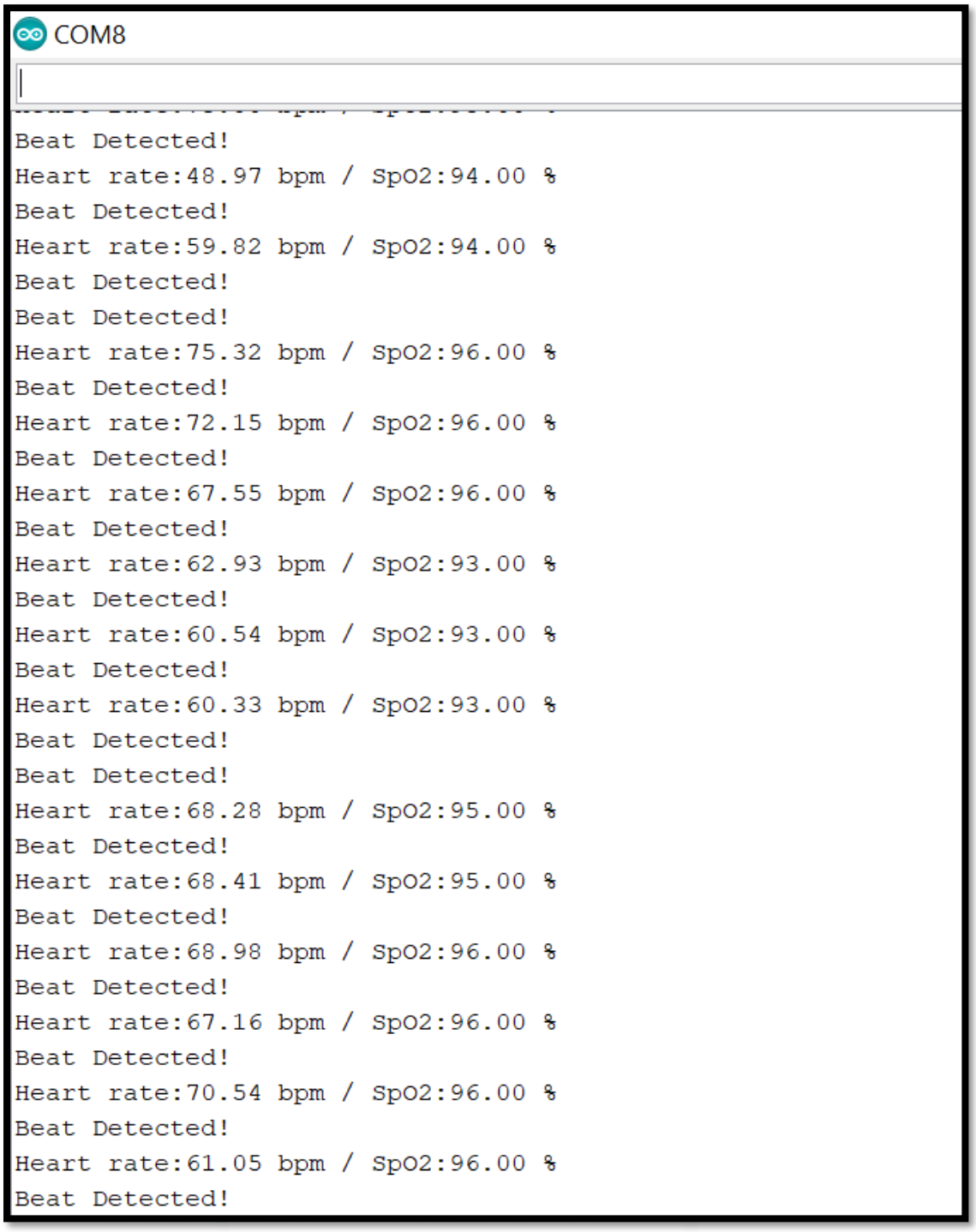


Fig.15:Output from Pulse Oximeter as shown in serial monitor

➢ SOURCECODE FOR ECG AD8232

```
#include <ESP8266WiFi.h>
#include <BlynkSimpleEsp8266.h>
#define BLYNK_PRINT Serial
char auth[] = "wTY9Evzq9JyHHs1HT3EduxuWtznD****";

/* WiFi credentials */
char ssid[] = "D-Link_PRASUN";
char pass[] = "12345";
float ecg;

void setup() {
 // put your setup code here, to run once:
 Serial.begin(115200);
 Blynk.begin(auth, ssid, pass);
}
void loop() {
 // put your main code here, to run repeatedly:
 Blynk.run();
 ecg = analogRead(A0);
  Blynk.virtualWrite(V0,ecg);
Serial.println(analogRead(A0));
}
```

Output-

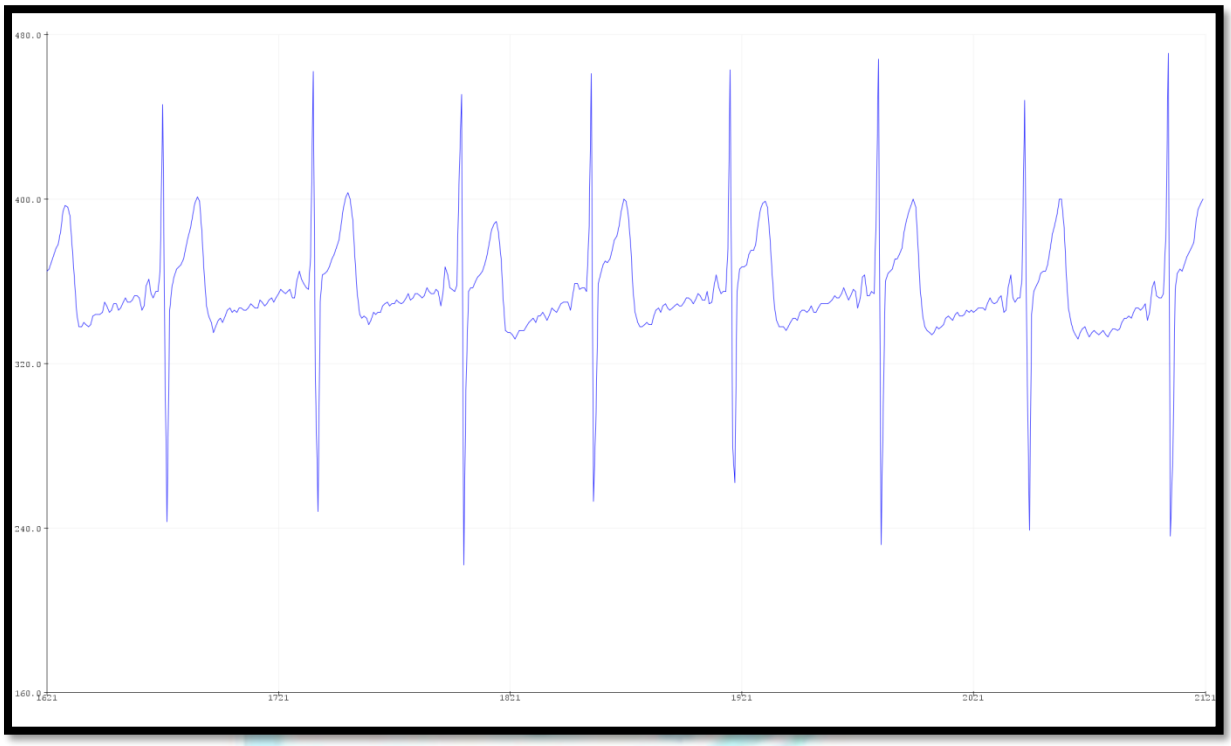


Fig.16: Output from ECG Module as shown in serial plotter

➢ FINAL CODE FOR THE MERGED CIRCUIT

```
#include <BlynkSimpleEsp8266.h>
#include <SimpleTimer.h>
#include <OneWire.h>
#include <DallasTemperature.h>
#include "MAX30100_PulseOximeter.h"
#include <ESP8266WiFi.h>
#include <Wire.h>

#define BLYNK_PRINT Serial
```

```
char auth[] = "wTY9Evzq9JyHHs1HT3EduxuWtznDZbTc";

/* WiFi credentials */
char ssid[] = "D-Link_PRASUN";
char pass[] = "PrasunP@230#";

SimpleTimer timer;
PulseOximeter pox;
float BPM, SpO2;
float ecg;
uint32_t tsLastReport = 0;
#define REPORTING_PERIOD_MS 1000
#define ONE_WIRE_BUS 2
OneWire oneWire(ONE_WIRE_BUS);
DallasTemperature DS18B20(&oneWire);
float temp;
float Fahrenheit=0;

void onBeatDetected()
{
   Serial.println("Beat Detected!");
}
void setup()
{
 Serial.begin(115200);
 Blynk.begin(auth, ssid, pass);
 DS18B20.begin();
    Serial.print("Initializing Pulse Oximeter..");

 timer.setInterval(1000L, getSendData);
```

```
if (!pox.begin())
   {
       Serial.println("FAILED");

   }
   else
   {
       Serial.println("SUCCESS");
   }
   pox.setIRLedCurrent(MAX30100_LED_CURR_7_6MA);
   pox.setOnBeatDetectedCallback(onBeatDetected);
}

void loop()
{
  timer.run(); // Initiates SimpleTimer
  ecg = analogRead(A0);
 Blynk.run();

pox.update();

   if (millis() - tsLastReport > REPORTING_PERIOD_MS)
   {
         BPM = pox.getHeartRate();
      SpO2 = pox.getSpO2();
      Serial.print("Heart rate:");
      Serial.print(BPM);
      Serial.print(" bpm / SpO2:");
      Serial.print(SpO2);
```

```
      Serial.println(" %");

      Blynk.virtualWrite(V7, BPM);
      Blynk.virtualWrite(V8, SpO2);

      tsLastReport = millis();
   }
Blynk.virtualWrite(V0,ecg);
Serial.println(analogRead(A0));
}

void getSendData()
{

 DS18B20.requestTemperatures();
 //Serial.print("Celsius:") ;
 temp = DS18B20.getTempCByIndex(0); // Celcius
 Fahrenheit = DS18B20.toFahrenheit(temp); // Fahrenheit
 Serial.println(temp);
 //Serial.println(Fahrenheit);
 Blynk.virtualWrite(V3, temp);
}
```

Output-

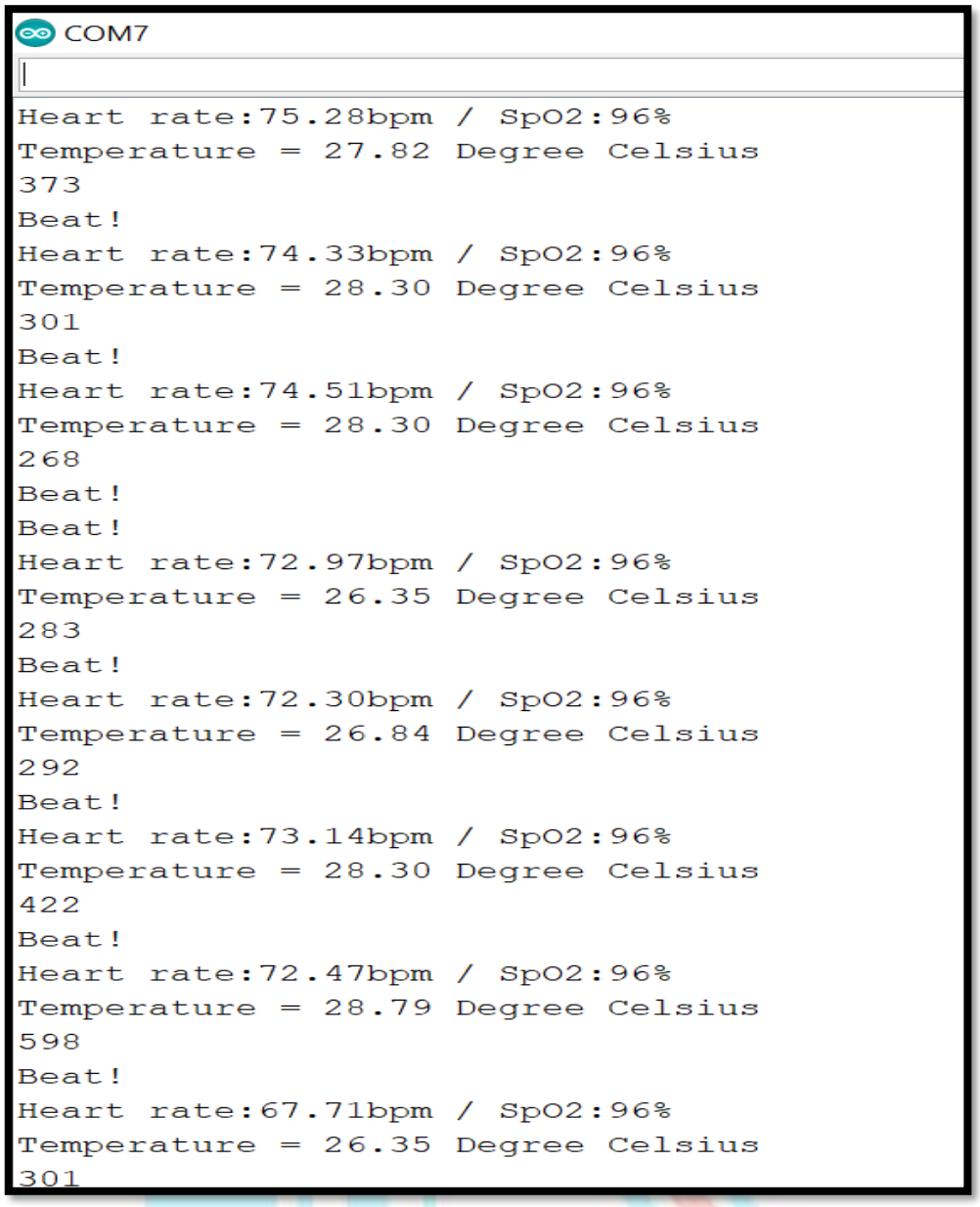


Fig.17: Output from all three sensors as shown in serial monitor

UPLOADING DATA TO CLOUD

- BLynk application has very easy user interface and hence can prove to be useful for family members as well as doctors to monitor the data easily and give medication accordingly.
- It uses the TCP/IP protocol which securely communicates with the respective known device and transfers the data in real time.
- Blynk application has different widgets which can be used limitedly and most importantly can be used with different microcontrollers such as Arduino, NodeMCU, Raspberry pi and the like.
- The interfacing of adding different widgets and creating its functionality is really very simple for non-tech people as well. Moreover, for long term application, one can also take the values in the csv files which can be used in the machine learning algorithm to predict and also analyse the data.
- There are two major ways of displaying sensor data in the app:

  PULL: In this case, Blynk app will request the data only when the app is open;

  PUSH: In this case the hardware will be constantly sending data to the Blynk Cloud. And when we open the app, it will be there waiting.

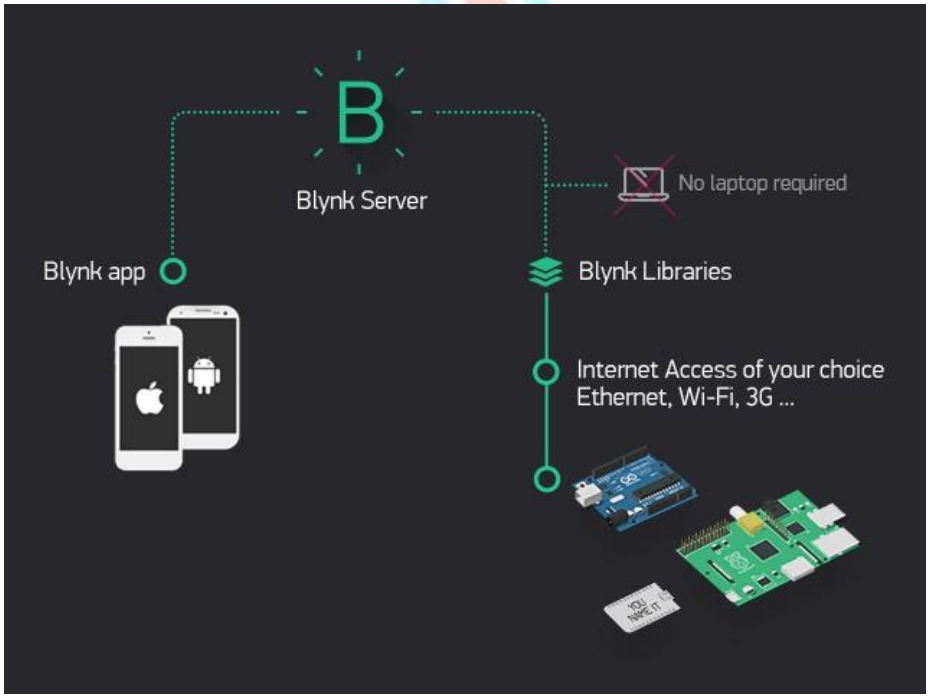
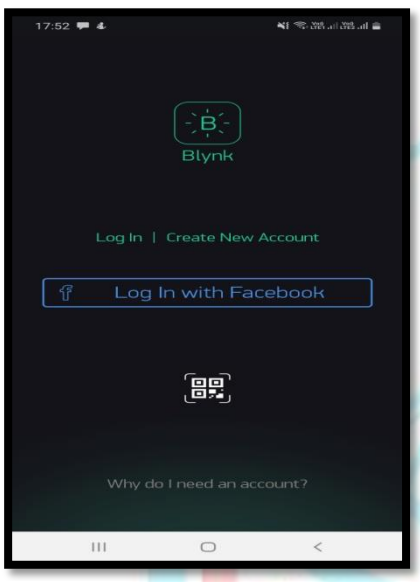
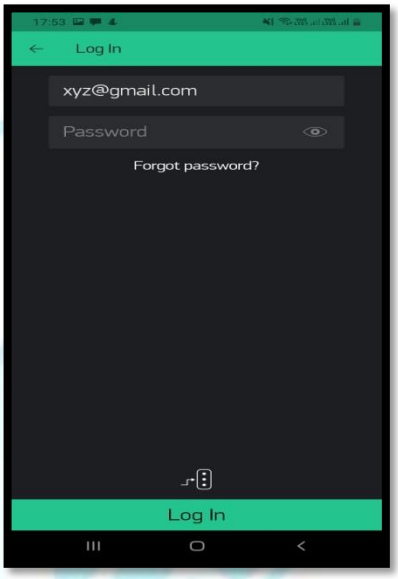


Fig.18: Overview of uploading data to cloud using Blynk

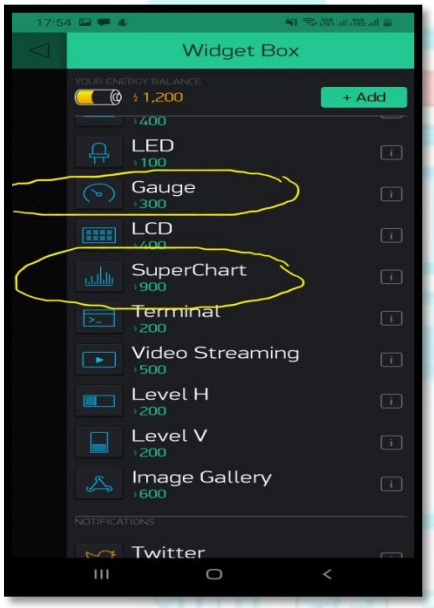
The process to collect and display the data on the Blynk application can be stated in the following simple steps:

1. Create a New Project after creating an account or log in using Face book (Fig-19)

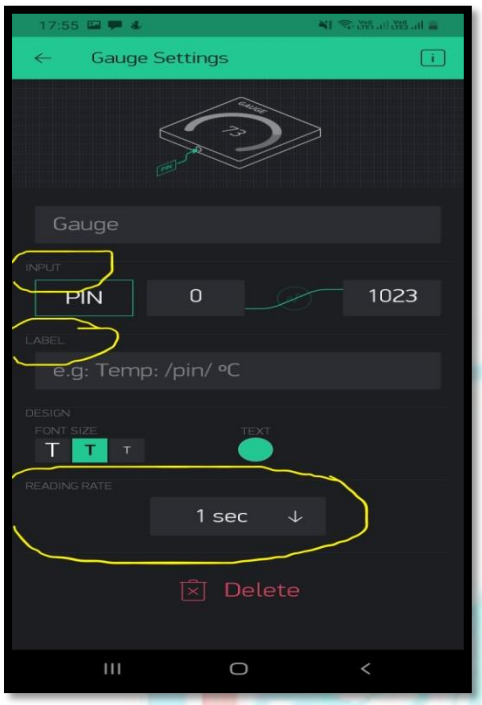




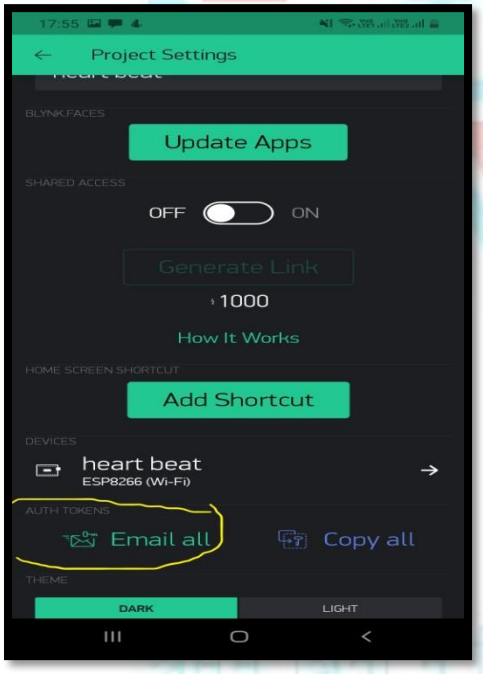
2. Add Value Display Widget such as gauge and super chart



3. After clicking the widgets go to particular widget Settings
4. Set PIN to Virtual Pin or analog/digital based on your sensor.
5. Set a Frequency of interval or set it to PUSH.



6. Open the coding sketch. Change pin respectively as mentioned in Blynk .
7. Send the auth taken to your email by clicking here.



8. Insert your Auth Token in the sketch
9. Flash the code to your microcontroller.
10. Go to the Blynk app - press **Play** button
11. Hurray ! The Real time data is updating and can be seen on the application.

OBSERVATIONS AND RESULTS

- ***Observation in BLYNK APP:*** The body parameters (body temperature, heart beat in BPM, oxygen rate in blood and ECG of the heart) of the patient are visible remotely on the Blynk app from any location.

Fig.20: Measured body parameters displayed remotely on Blynk App

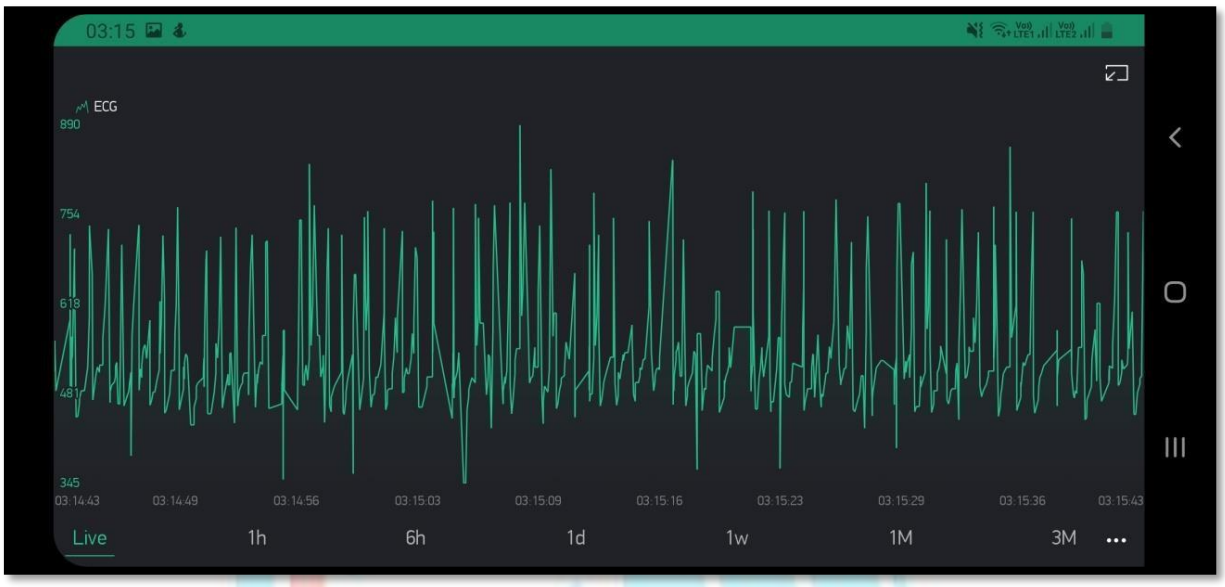


Fig.21: The ECG visualized separately on Blynk

- ***Analysis of the ECG:*** Body parameters of a healthy volunteer were obtained using our E-Health monitoring system. ECG plot parts were traced out and compared with normal range of ECG parameters.

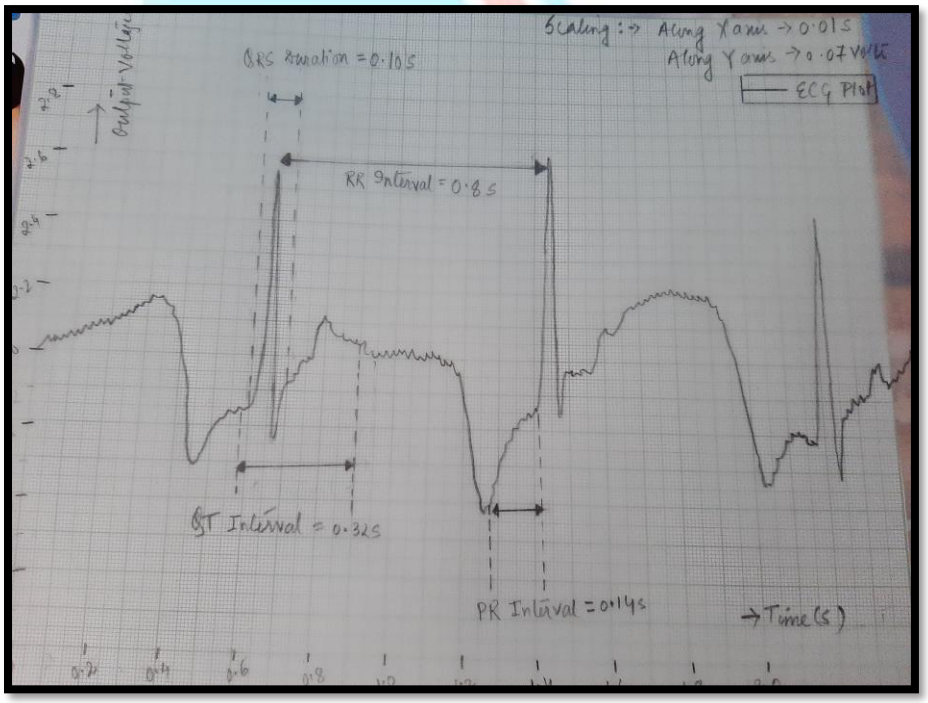


Fig.22: Traced out ECG plot part as obtained by our prototype

NORMAL VALUES OF KEY ECG PARATERMS.

Features	Normal range (Second)
RR interval	0.6- 1
PR interval	0.12- 0.20
QT interval	0.32- 0.44
QRS duration	< 0.12

Fig.23: Normal parameter ranges of ECG wave

Studying the plot obtained, we come to the following analysis:

REPORT-

RR interval – Normal (0.8s)

PR interval – Normal (0.14s)

QT interval – Normal(0.32s)

QRS Duration – Normal (0.10s)

Hence, the ECG is normal without any abnormal parameters.

ABNORMAL PARAMETERS:-

1) Increased or decreased P waves can indicate problems with the potassium ion concentration in the body that will alter nerve activity.

2) A missing P wave indicates atrial fibrillation, a cardiac arrhythmia in which the heart beats irregularly, preventing efficient ventricular diastole.

3) Abnormalities in the QRS complex may indicate cardiac hypertrophy or myocardial infarctions.

4) An elevated ST segment is the classic indicator for myocardial infarctions, though missing or downward sloping ST segments may indicate myocardial ischemia.

CONCLUSION

In this project, we designed and developed an E-Health Monitoring System using IoT. This prototype was designed keeping in mind the problems faced by most of the people who deal with tight daily schedules and tend to postpone or miss their required health check-ups. This system can also provide assistance to the elderly people who find it inconvenient and difficult to visit clinics or diagnostic centers for their regular check-ups. With the help of the remote monitoring system provided by our prototype, health monitoring can be done by the doctors or health care providers at anytime from any location in a cost effective manner. As this system size is quite small so it can be carried at various locations with ease. Through the use of small circuitry the heartbeat and ECG signals of a patient can be viewed rather than using large machines for it.

Doctors can see data remotely and analyze the health parameters of patients. This is the most important advantage of this system. The persons living in remote locations who have no access to a doctor can be helped through a greater extent through this system, as this system sends all the values and signals on the website and the doctors which are far away can get an accurate idea of heart condition of a person. Furthermore this system can be used in ambulance which saves a lot of time and can save a life of a person because every second counts.

It is evident that the implementation of such a system will help in early detection of abnormal conditions of cardiovascular diseases and prevention of its serious consequences.

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SPECIFICATIONS OF HARDWARE COMPONENETS-

ESPRESSIF SMART CONNECTIVITY PLATFORM: ESP8266

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Table of Contents

1 Introduction

Espressif Systems' Smart Connectivity Platform (ESCP) of high performance wireless SOCs, for mobile platform designers, provides unsurpassed ability to embed Wi-Fi capabilities within other systems, at the lowest cost with the greatest functionality.

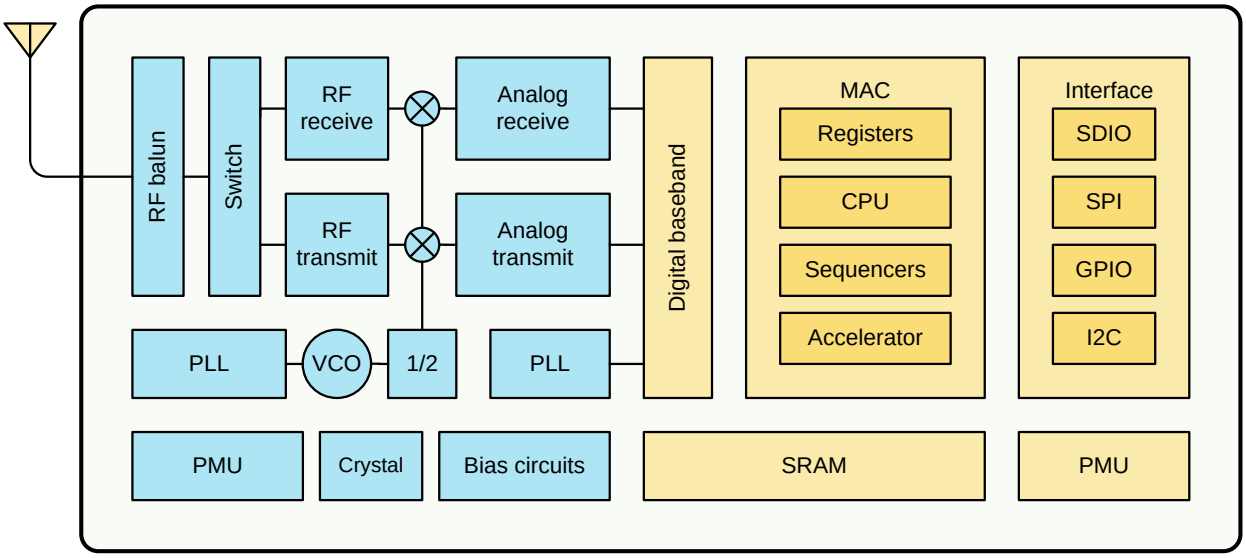


Figure 1: ESP8266 Block Diagram

2 Technology Overview

ESP8266 offers a complete and self-contained Wi-Fi networking solution, allowing it to either host the application or to offload all Wi-Fi networking functions from another application processor.

When ESP8266 hosts the application, and when it is the only application processor in the device, it is able to boot up directly from an external flash. It has integrated cache to improve the performance of the system in such applications, and to minimize the memory requirements.

Alternately, serving as a Wi-Fi adapter, wireless internet access can be added to any microcontroller-based design with simple connectivity through UART interface or the CPU AHB bridge interface.

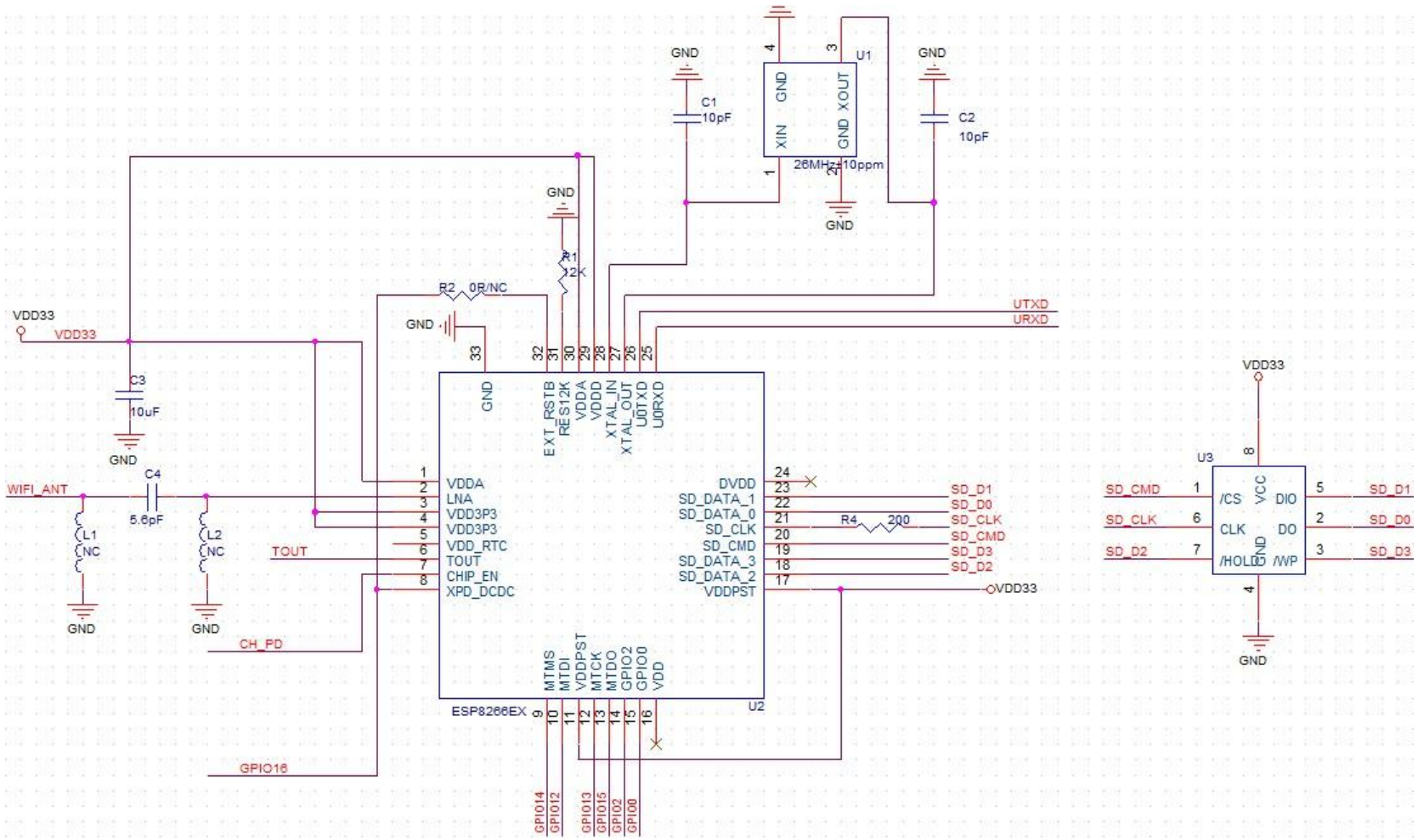
ESP8266 on-board processing and storage capabilities allow it to be integrated with the sensors and other application specific devices through its GPIOs with minimal development up-front and minimal loading during runtime. With its high degree of on-chip integration, which includes the antenna switch balun, power management converters, it requires minimal external circuitry, and the entire solution, including front-end module, is designed to occupy minimal PCB area.

Sophisticated system-level features include fast sleep/wake context switching for energy-efficient VoIP, adaptive radio biasing for low-power operation, advance signal processing, and spur cancellation and radio co-existence features for common cellular, Bluetooth, DDR, LVDS, LCD interference mitigation.

3 Features

- 802.11 b/g/n protocol
- Wi-Fi Direct (P2P), soft-AP
- Integrated TCP/IP protocol stack
- Integrated TR switch, balun, LNA, power amplifier and matching network
- Integrated PLL, regulators, and power management units
- +19.5dBm output power in 802.11b mode
- Integrated temperature sensor
- Supports antenna diversity
- Power down leakage current of < 10uA
- Integrated low power 32-bit CPU could be used as application processor
- SDIO 2.0, SPI, UART
- STBC, 1×1 MIMO, 2×1 MIMO
- A-MPDU & A-MSDU aggregation & 0.4μs guard interval
- Wake up and transmit packets in < 2ms
- Standby power consumption of < 1.0mW (DTIM3)

4 Application Diagram



5 Ultra Low Power Technology

ESP8266 has been designed for mobile, wearable electronics and Internet of Things applications with the aim of achieving the lowest power consumption with a combination of several proprietary techniques. The power saving architecture operates in 3 modes: active mode, sleep mode and deep sleep mode.

By using advance power management techniques and logic to power-down functions not required and to control switching between sleep and active modes, ESP8266 consumes less than 12uA in sleep mode and less than 1.0mW (DTIM=3) or less than 0.5mW (DTIM=10) to stay connected to the access point.

When in sleep mode, only the calibrated real-time clock and watchdog remains active. The real-time clock can be programmed to wake up the ESP8266 at any required interval.

The ESP8266 can be programmed to wake up when a specified condition is detected. This minimal wake-up time feature of the ESP8266 can be utilized by mobile device SOCs, allowing them to remain in the low-power standby mode until Wi-Fi is needed.

In order to satisfy the power demand of mobile and wearable electronics, ESP8266 can be programmed to reduce the output power of the PA to fit various application profiles, by trading off range for power consumption.

5.1 Highest Level of Integration

By integrating the costliest components such as power management unit, TR switch, RF balun, high power PA capable of delivering +25dBm (peak), ESP8266 ensures that the BOM cost is the lowest possible, and ease of integration into any system.

With ESP8266, the only external BOM are resistors, capacitors, and crystal.

6 ESP8266 Applications

- Smart power plugs
- Home automation
- Mesh network
- Industrial wireless control
- Baby monitors
- IP Cameras
- Sensor networks
- Wearable electronics
- Wi-Fi location-aware devices
- Security ID tags
- Wi-Fi position system beacons

7 Specifications

7.1 Current Consumption

The following current consumption is based on 3.3V supply, and 25°C ambient, using internal regulators. Measurements are done at antenna port without SAW filter. All the transmitter's measurements are based on 90% duty cycle, continuous transmit mode.

Mode	Min	Typ	Max	Unit
Transmit 802.11b, CCK 1Mbps, P_{OUT}=+19.5dBm		215		mA
Transmit 802.11b, CCK 11Mbps, P_{OUT}=+18.5dBm		197		mA
Transmit 802.11g, OFDM 54Mbps, P_{OUT} =+16dBm		145		mA
Transmit 802.11n, MCS7, P_{OUT}=+14dBm		135		mA
Receive 802.11b, packet length=1024 byte, -80dBm		60		mA
Receive 802.11g, packet length=1024 byte, -70dBm		60		mA
Receive 802.11n, packet length=1024 byte, -65dBm		62		mA
Standby		0.9		mA
Deep sleep		10		uA
Power save mode DTIM 1		1.2		mA
Power save mode DTIM 3		0.86		mA
Total shutdown		0.5		uA

7.2 RF Performance

The following are measured under room temperature conditions with 3.3V and 1.1V power supplies.

Description	Min	Typical	Max	Unit
Input frequency	2412		2484	MHz
Input impedance		50		Ω
Input reflection			-10	dB
Output power of PA for 72.2Mbps	14	15	16	dBm
Output power of PA for 11b mode	17.5	18.5	19.5	dBm
Sensitivity				
CCK, 1Mbps		-98		dBm
CCK, 11Mbps		-91		dBm
6Mbps (1/2 BPSK)		-93		dBm
54Mbps (3/4 64-QAM)		-75		dBm
HT20, MCS7 (65Mbps, 72.2Mbps)		-71		dBm
Adjacent Channel Rejection				
OFDM, 6Mbps		37		dB
OFDM, 54Mbps		21		dB
HT20, MCS0		37		dB
HT20, MCS7		20		dB

8 CPU, Memory and Interfaces

8.1 CPU

This chip embeds an ultra low power Micro 32-bit CPU, with 16-bit thumb mode. This CPU can be interfaced using:

- code RAM/ROM interface (iBus) that goes to the memory controller, that can also be used to access external flash memory,
- data RAM interface (dBus), that also goes to the memory controller
- AHB interface, for register access, and
- JTAG interface for debugging

8.2 Memory Controller

The memory controller contains ROM, and SRAM. It is accessed by the CPU using the iBus, dBus and AHB interface. Any of these interfaces can request access to the ROM or RAM modules, and the memory controller arbiters serve these 3 interfaces on a first-come-first-serve basis.

8.3 AHB and AHB Blocks

The AHB blocks performs the function of an arbiter, controls the AHB interfaces from the MAC, SDIO (host) and CPU. Depending on the address, the AHB data requests can go into one of the two slaves:

- APB block, or
- flash controller (usually for standalone applications).

Data requests to the memory controller are usually high speed requests, and requests to the APB block are usually register access.

The APB block acts as a decoder. It is meant only for access to programmable registers within ESP8266's main blocks. Depending on the address, the APB request can go to the radio, SI/SPI, SDIO (host), GPIO, UART, real-time clock (RTC), MAC or digital baseband.

8.4 Interfaces

The ESP8266 contains several analog and digital interfaces described in the following sections.

8.4.1 Master SI / SPI Control (Optional)

The master serial interface (SI) can operate in two, three or four-wire bus configurations to control the EEPROM or other I2C/SPI devices. Multiple I2C devices with different device addresses are supported by sharing the 2-wire bus.

Multiple SPI devices are supported by sharing the clock and data signals, using separate software controlled GPIO pins as chip selects.

The SPI can be used for controlling external devices such as serial flash memories, audio CODECs, or other slave devices. It is set up as a standard master SPI device with 3 different enable pins:

- SPI_EN0,
- SPI_EN1,
- SPI_EN2.

Both SPI master and SPI slave are supported with the latter being used as a host interface.

SPI_EN0 is used as an enable signal to an external serial flash memory for downloading patch code and/or MIB-data to the baseband in an embedded application. In a host based application, patch code and MIB-data can alternatively be downloaded via the host interface. This pin is active low and should be left open if not used.

SPI_EN1 is usually used for a user application, e.g. to control an external audio codec or sensor ADC, in an embedded application. This pin is active low and should be left open if not used.

SPI_EN2 usually controls an EEPROM to store individual data, such as MIB information, MAC address, and calibration data, or for general use. This pin is active low and should be left open if not used.

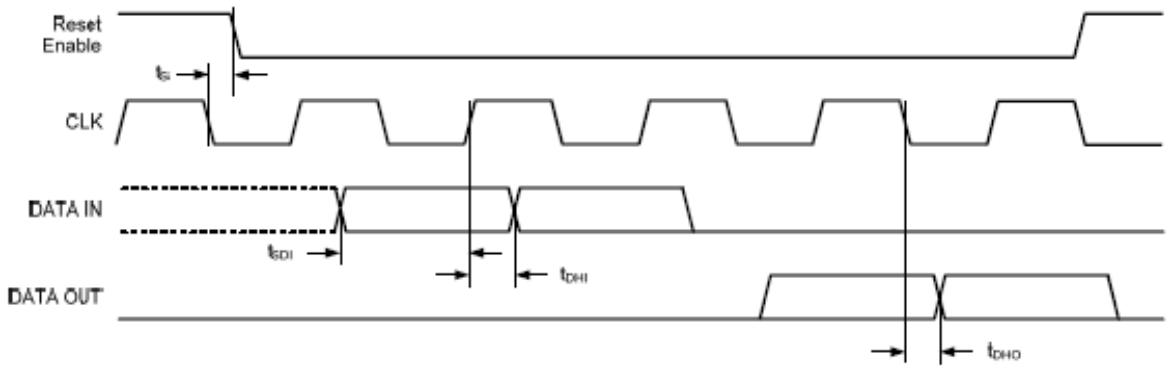


Figure 2: SPI timing characteristics

8.4.2 General Purpose IO

There are up to 16 GPIO pins. They can be assigned to various functions by the firmware. Each GPIO can be configured with internal pull-up/down, input available for sampling by a software register, input triggering an edge or level CPU interrupt, input triggering a level wakeup interrupt, open-drain or push-pull output driver, or output source from a software register, or a sigma-delta PWM DAC.

These pins are multiplexed with other functions such as host interface, UART, SI, Bluetooth coexistence, etc.

8.4.3 Digital IO Pads

The digital IO pads are bidirectional, non-inverting and tri-state. It includes input and an output buffer with tristate control inputs. Besides this, for low power operations, the IO can also be set to hold. For instance, when we power down the chip, all output enable signals can be set to hold low.

Optional hold functionality can be built into the IO if requested. When the IO is not driven by the internal or external circuitry, the hold functionality can be used to hold the state to the last used state.

The hold functionality introduces some positive feedback into the pad. Hence, the external driver that drives the pad must be stronger than the positive feedback. The required drive strength is however small – in the range of 5uA.

Parameter	Symbol	Min	Max	Unit
Input low voltage	**V_{IL}**	**-0.3**	**$0.25 \times V_{IO}$**	**V**
Input high voltage	**V_{IH}**	**0.75×VIO**	**3.6**	**V**
Input leakage current	**I_{IL}**		**50**	**nA**
Output low voltage	**V_{OL}**		**$0.1 \times V_{IO}$**	**V**
Output high voltage	**V_{OH}**	**0.8×VIO**		**V**
Input pin capacitance	**C_{pad}**		**2**	**pF**
VDDIO	**V_{IO}**	**1.7**	**3.6**	**V**
Maximum drive capability	**I_{MAX}**		**12**	**mA**
Temperature	**T_{amb}**	**-20**	**100**	**°C**

All digital IO pins are protected from over-voltage with a snap-back circuit connected between the pad and ground. The snap back voltage is typically about 6V, and the holding voltage is 5.8V. This provides protection from over-voltages and ESD. The output devices are also protected from reversed voltages with diodes.

9 Firmware & Software Development Kit

The application and firmware is executed in on-chip ROM and SRAM, which loads the instructions during wake-up, through the SDIO interface, from the external flash.

The firmware implements TCP/IP, the full 802.11 b/g/n/e/i WLAN MAC protocol and Wi-Fi Direct specification. It supports not only basic service set (BSS) operations under the distributed control function (DCF) but also P2P group operation compliant with the latest Wi-Fi P2P protocol. Low level protocol functions are handled automatically by ESP8266:

- RTS/CTS,
- acknowledgement,
- fragmentation and defragmentation,
- aggregation,
- frame encapsulation (802.11h/RFC 1042),
- automatic beacon monitoring / scanning, and
- P2P Wi-Fi direct,

Passive or active scanning, as well as P2P discovery procedure is performed autonomously once initiated by the appropriate command. Power management is handled with minimum host interaction to minimize active duty period.

9.1 Features

The SDK includes the following library functions:

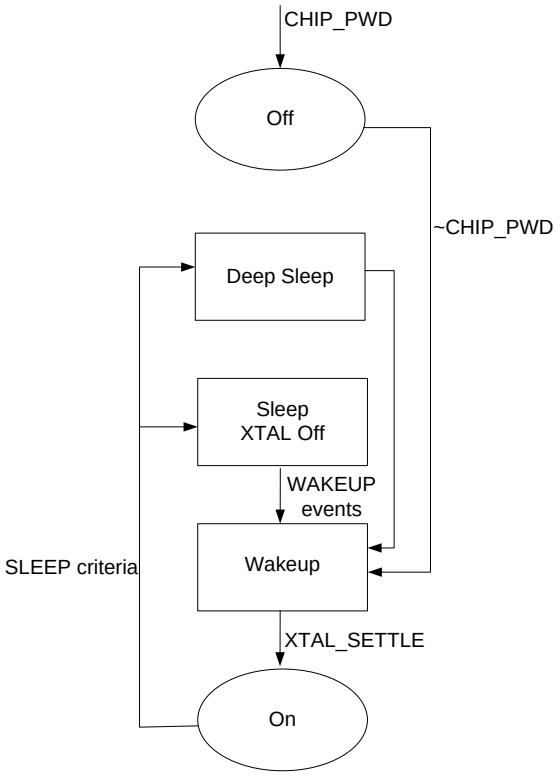
- 802.11 b/g/n/d/e/i/k/r support;
- Wi-Fi Direct (P2P) support:
- P2P Discovery, P2P Group Owner mode, P2P Power Management
- Infrastructure BSS Station mode / P2P mode / softAP mode support;
- Hardware accelerators for CCMP (CBC-MAC, counter mode), TKIP (MIC, RC4), WAPI (SMS4), WEP (RC4), CRC;

- WPA/WPA2 PSK, and WPS driver;
- Additional 802.11i security features such as pre-authentication, and TSN;
- Open Interface for various upper layer authentication schemes over EAP such as TLS, PEAP, LEAP, SIM, AKA, or customer specific;
- 802.11n support (2.4GHz / 5GHz);
- Supports MIMO 1×1 and 2×1, STBC, A-MPDU and A-MSDU aggregation and 0.4μs guard interval;
- WMM power save U-APSD;
- Multiple queue management to fully utilize traffic prioritization defined by 802.11e standard;
- UMA compliant and certified;
- 802.1h/RFC1042 frame encapsulation;
- Scattered DMA for optimal CPU off load on Zero Copy data transfer operations;
- Antenna diversity and selection (software managed hardware);
- Clock/power gating combined with 802.11-compliant power management dynamically adapted to curent connection condition providing minimal power consumption;
- Adaptive rate fallback algorithm sets the optimium transmission rate and Tx power based on actual SNR and packet loss information;
- Automatic retransmission and response on MAC to avoid packet discarding on slow host environment;
- Seamless roaming support;
- Configurable packet traffic arbitration (PTA) with dedicated slave processor based design provides flexible and exact timing Bluetooth co-existence supoport for a wide range of Bluetooth Chip vendors;
- Dual and single antenna Bluetooth co-existence support with optional simultaneous receive (Wi-Fi/Bluetooth) capability.

10 Power Management

The chip can be put into the following states:

- **OFF**: CHIP_PD pin is low. The RTC is disabled. All registers are cleared.
- **DEEP_SLEEP**: Only RTC is powered on – the rest of the chip is powered off. Recovery memory of RTC can keep basic Wi-Fi connecting information.
- **SLEEP**: Only the RTC is operating. The crystal oscillator is disabled. Any wakeup events (MAC, host, RTC timer, external interrupts) will put the chip into the WAKEUP state.
- **WAKEUP**: In this state, the system goes from the sleep states to the PWR state. The crystal oscillator and PLLs are enabled.



- **ON state**: the high speed clock is operational and sent to each block enabled by the clock control register. Lower level clock gating is implemented at the block level, including the CPU, which can be gated off using the WAITI instruction, while the system is on.

11 Clock Management

11.1 High Frequency Clock

The high frequency clock on ESP8266 is used to drive both the Tx and Rx mixers. This clock is generated from the internal crystal oscillator and an external crystal. The crystal frequency can range from 26MHz to 52MHz.

While internal calibration of the crystal oscillator ensures that a wide range of crystals can be used, in general, the quality of the crystal is still a factor to consider, to obtain reasonable phase noise. When the crystal selected is sub-optimal due to large frequency drifts or poor Q-factor, the maximum throughput and sensitivity of the Wi-Fi system is degraded. Please refer to the application notes on how the frequency offset can be measured.

Parameter	Symbol	Min	Max	Unit
Frequency	F_{XO}	26	52	MHz
Loading capacitance	C_L		32	pF
Motional capacitance	C_M	2	5	pF
Series resistance	R_S	0	65	Ω
Frequency tolerance	ΔF_{XO}	-15	15	ppm
Frequency vs temperature (-25°C ~ 75°C)	$\Delta F_{XO,Temp}$	-15	15	ppm

11.2 External Reference Requirements

For an externally generated clock, the frequency can range from 26MHz to 52MHz can be used.

For good performance of the radio, the following characteristics are expected of the clock:

Parameter	Symbol	Min	Max	Unit
Clock amplitude	V_{XO}	0.2	1	Vpp
External clock accuracy	$\Delta F_{XO,EXT}$	-15	15	ppm
Phase noise @1kHz offset, 40MHz clock			-120	dBc/Hz
Phase noise @10kHz offset, 40MHz clock			-130	dBc/Hz
Phase noise @100kHz offset, 40MHz clock			-138	dBc/Hz

12 Radio

The ESP8266 radio consists of the following main blocks:

- 2.4GHz receiver
- 2.4GHz transmitter
- High speed clock generators and crystal oscillator
- Real time clock
- Bias and regulators
- Power management

12.1 Channel Frequencies

The RF transceiver supports the following channels according to the IEEE802.11bgn standards.

Channel No	Frequency (MHz)	Channel No	Frequency (MHz)
1	2412	8	2447
2	2417	9	2452
3	2422	10	2457
4	2427	11	2462
5	2432	12	2467
6	2437	13	2472
7	2442	14	2484

12.2 2.4GHz Receiver

The 2.4GHz receiver downconverts the RF signal to quadrature baseband signals and converts them to the digital domain with 2 high resolution high speed ADCs. To adapt to varying signal channel conditions, RF filters, automatic gain control, DC offset cancelation circuits and baseband filters are integrated within the radio.

12.3 2.4GHz Transmitter

The 2.4GHz transmitter upconverts the quadrature baseband signals to 2.4GHz, and drives the antenna with a high powered CMOS power amplifier. The use of digital calibration further improves the linearity of the power amplifier, enabling a state of art performance of delivering +19dBm average power for 802.11b transmission and +16dBm for 802.11n transmission.

Additional calibrations are integrated to cancel any imperfections of the radio, such as:

- carrier leakage,
- I/Q phase matching, and
- baseband nonlinearities

This reduces the amount of time required and test equipment required for production testing.

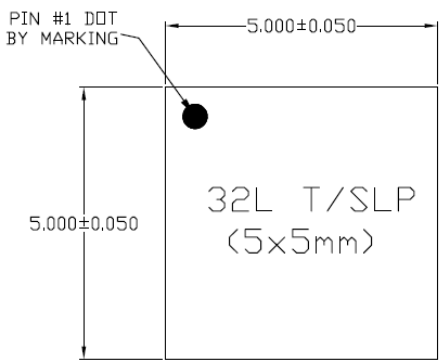
12.4 Clock Generator

The clock generator generates quadrature 2.4GHz clock signals for the receiver and transmitter. All components of the clock generator are integrated on-chip, including:

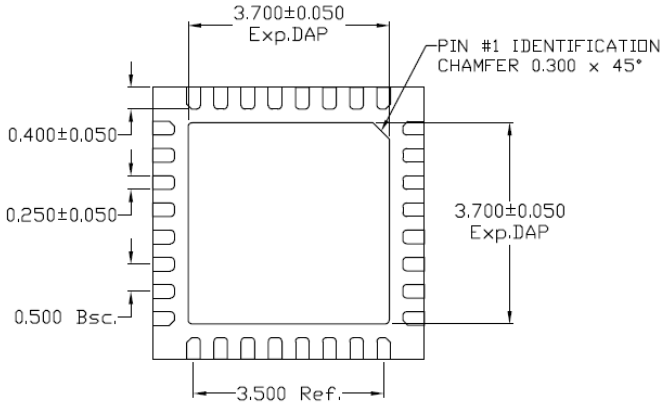
- inductor,
- varactor, and
- loop filter.

The clock generator has built-in calibration and self test circuits. Quadrature clock phases and phase noise are optimized on-chip with patented calibration algorithms to ensure the best receiver and transmitter performance.

App. QFN32 Package Drawing



TOP VIEW

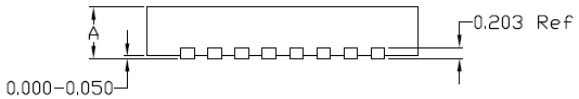


BOTTOM VIEW

NOTE:

1) TSLP AND SLP SHARE THE SAME EXPOSE OUTLINE BUT WITH DIFFERENT THICKNESS:

		TSLP	SLP
A	MAX.	0.800	0.900
	NOM.	0.750	0.850
	MIN.	0.700	0.800



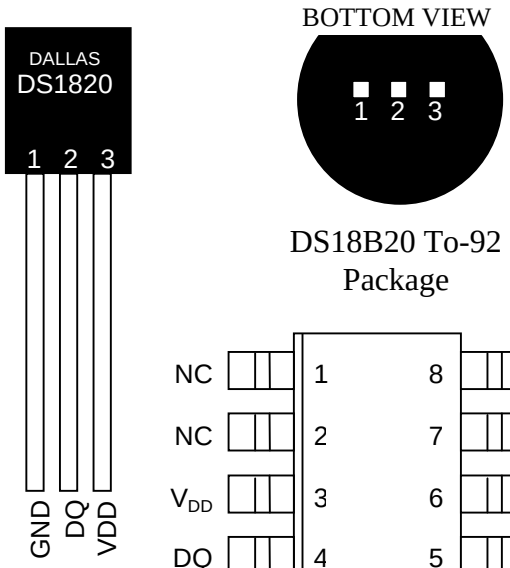
SIDE VIEW

DS18B20
Programmable Resolution 1-Wire® Digital Thermometer

FEATURES

- Unique 1-Wire interface requires only one port pin for communication
- Multidrop capability simplifies distributed temperature sensing applications
- Requires no external components
- Can be powered from data line. Power supply range is 3.0V to 5.5V
- Zero standby power required
- Measures temperatures from -55°C to +125°C. Fahrenheit equivalent is -67°F to +257°F
- ±0.5°C accuracy from -10°C to +85°C
- Thermometer resolution is programmable from 9 to 12 bits
- Converts 12-bit temperature to digital word in 750 ms (max.)
- User-definable, nonvolatile temperature alarm settings
- Alarm search command identifies and addresses devices whose temperature is outside of programmed limits (temperature alarm condition)
- Applications include thermostatic controls, industrial systems, consumer products, thermometers, or any thermally sensitive system

PIN ASSIGNMENT



DS18B20 To-92 Package

DS18B20Z
8-Pin SOIC (150 mil)

PIN DESCRIPTION

GND - Ground
DQ - Data In/Out
V_{DD} - Power Supply Voltage
NC - No Connect

DESCRIPTION

The DS18B20 Digital Thermometer provides 9 to 12-bit (configurable) temperature readings which indicate the temperature of the device.

Information is sent to/from the DS18B20 over a 1-Wire interface, so that only one wire (and ground) needs to be connected from a central microprocessor to a DS18B20. Power for reading, writing, and performing temperature conversions can be derived from the data line itself with no need for an external power source.

Because each DS18B20 contains a unique silicon serial number, multiple DS18B20s can exist on the same 1-Wire bus. This allows for placing temperature sensors in many different places. Applications where this feature is useful include HVAC environmental controls, sensing temperatures inside buildings, equipment or machinery, and process monitoring and control.

DETAILED PIN DESCRIPTION Table 1

PIN 8PIN SOIC	PIN TO92	SYMBOL	DESCRIPTION
5	1	GND	Ground.
4	2	DQ	**Data Input/Output pin.** For 1-Wire operation: Open drain. (See "Parasite Power" section.)
3	3	V_{DD}	**Optional V_{DD} pin.** See "Parasite Power" section for details of connection. V_{DD} must be grounded for operation in parasite power mode.

DS18B20Z (8-pin SOIC): All pins not specified in this table are not to be connected.

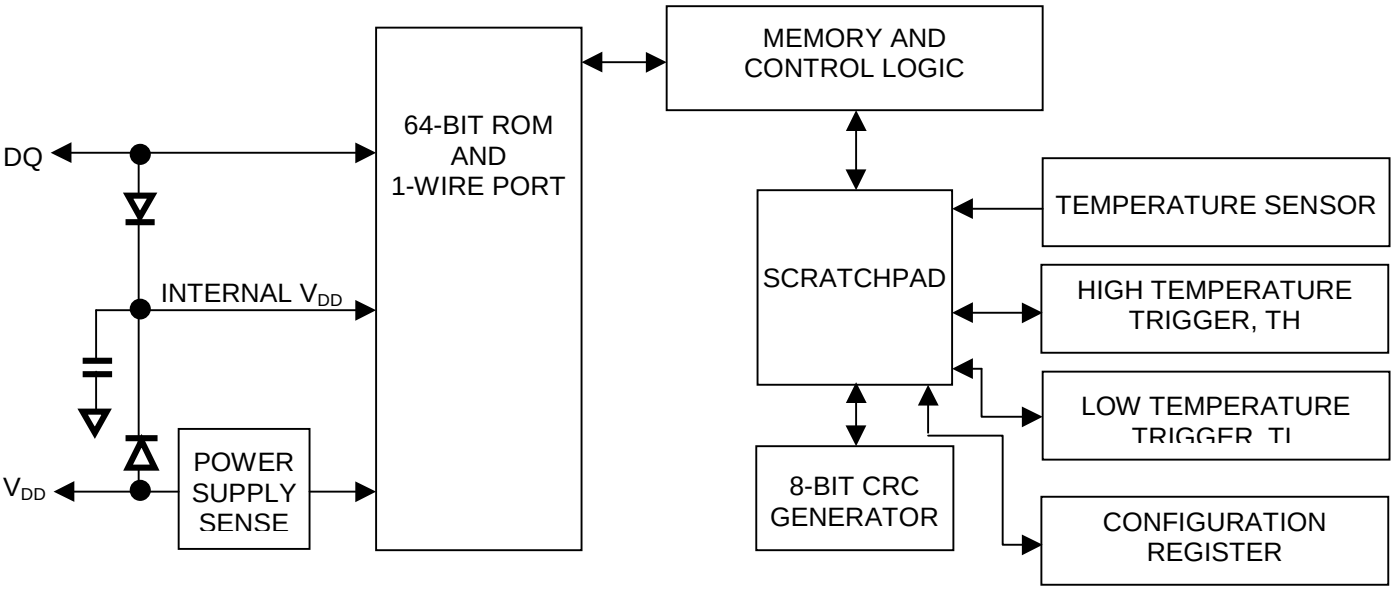
OVERVIEW

The block diagram of Figure 1 shows the major components of the DS18B20. The DS18B20 has four main data components: 1) 64-bit lasered ROM, 2) temperature sensor, 3) nonvolatile temperature alarm triggers TH and TL, and 4) a configuration register. The device derives its power from the 1-Wire communication line by storing energy on an internal capacitor during periods of time when the signal line is high and continues to operate off this power source during the low times of the 1-Wire line until it returns high to replenish the parasite (capacitor) supply. As an alternative, the DS18B20 may also be powered from an external 3 volt - 5.5 volt supply.

Communication to the DS18B20 is via a 1-Wire port. With the 1-Wire port, the memory and control functions will not be available before the ROM function protocol has been established. The master must first provide one of five ROM function commands: 1) Read ROM, 2) Match ROM, 3) Search ROM, 4) Skip ROM, or 5) Alarm Search. These commands operate on the 64-bit lasered ROM portion of each device and can single out a specific device if many are present on the 1-Wire line as well as indicate to the bus master how many and what types of devices are present. After a ROM function sequence has been successfully executed, the memory and control functions are accessible and the master may then provide any one of the six memory and control function commands.

One control function command instructs the DS18B20 to perform a temperature measurement. The result of this measurement will be placed in the DS18B20's scratch-pad memory, and may be read by issuing a memory function command which reads the contents of the scratchpad memory. The temperature alarm triggers TH and TL consist of 1 byte EEPROM each. If the alarm search command is not applied to the DS18B20, these registers may be used as general purpose user memory. The scratchpad also contains a configuration byte to set the desired resolution of the temperature to digital conversion. Writing TH, TL, and the configuration byte is done using a memory function command. Read access to these registers is through the scratchpad. All data is read and written least significant bit first.

DS18B20 BLOCK DIAGRAM Figure 1



PARASITE POWER

The block diagram (Figure 1) shows the parasite-powered circuitry. This circuitry "steals" power whenever the DQ or V_{DD} pins are high. DQ will provide sufficient power as long as the specified timing and voltage requirements are met (see the section titled "1-Wire Bus System"). The advantages of parasite power are twofold: 1) by parasiting off this pin, no local power source is needed for remote sensing of temperature, and 2) the ROM may be read in absence of normal power.

In order for the DS18B20 to be able to perform accurate temperature conversions, sufficient power must be provided over the DQ line when a temperature conversion is taking place. Since the operating current of the DS18B20 is up to 1.5 mA, the DQ line will not have sufficient drive due to the 5k pullup resistor. This problem is particularly acute if several DS18B20s are on the same DQ and attempting to convert simultaneously.

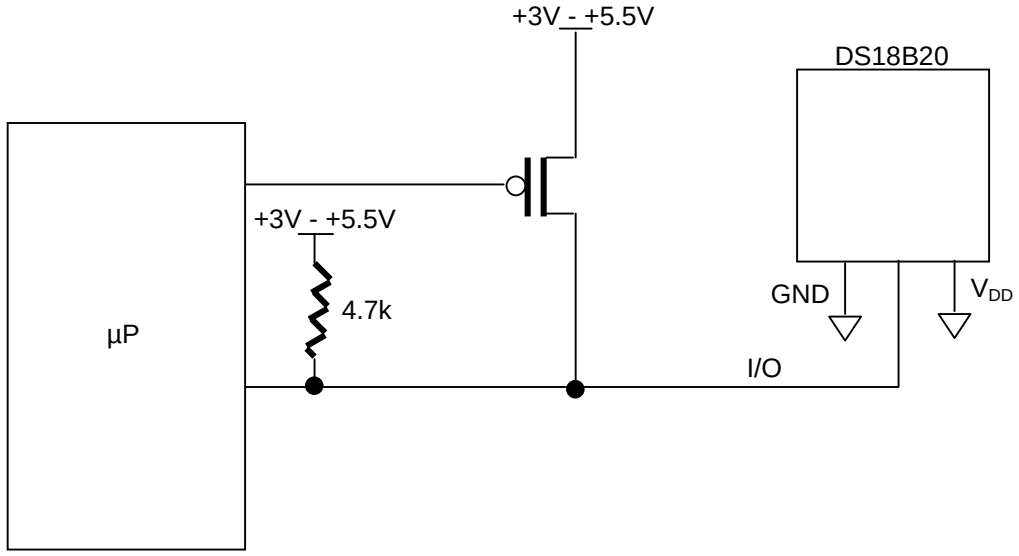
There are two ways to assure that the DS18B20 has sufficient supply current during its active conversion cycle. The first is to provide a strong pullup on the DQ line whenever temperature conversions or copies to the E^2 memory are taking place. This may be accomplished by using a MOSFET to pull the DQ line directly to the power supply as shown in Figure 2. The DQ line must be switched over to the strong pull-up within 10 µs maximum after issuing any protocol that involves copying to the E^2 memory or initiates temperature conversions. When using the parasite power mode, the V_{DD} pin must be tied to ground.

Another method of supplying current to the DS18B20 is through the use of an external power supply tied to the V_{DD} pin, as shown in Figure 3. The advantage to this is that the strong pullup is not required on the DQ line, and the bus master need not be tied up holding that line high during temperature conversions. This allows other data traffic on the 1-Wire bus during the conversion time. In addition, any number of DS18B20s may be placed on the 1-Wire bus, and if they all use external power, they may all simultaneously perform temperature conversions by issuing the Skip ROM command and then issuing the Convert T command. Note that as long as the external power supply is active, the GND pin may not be floating.

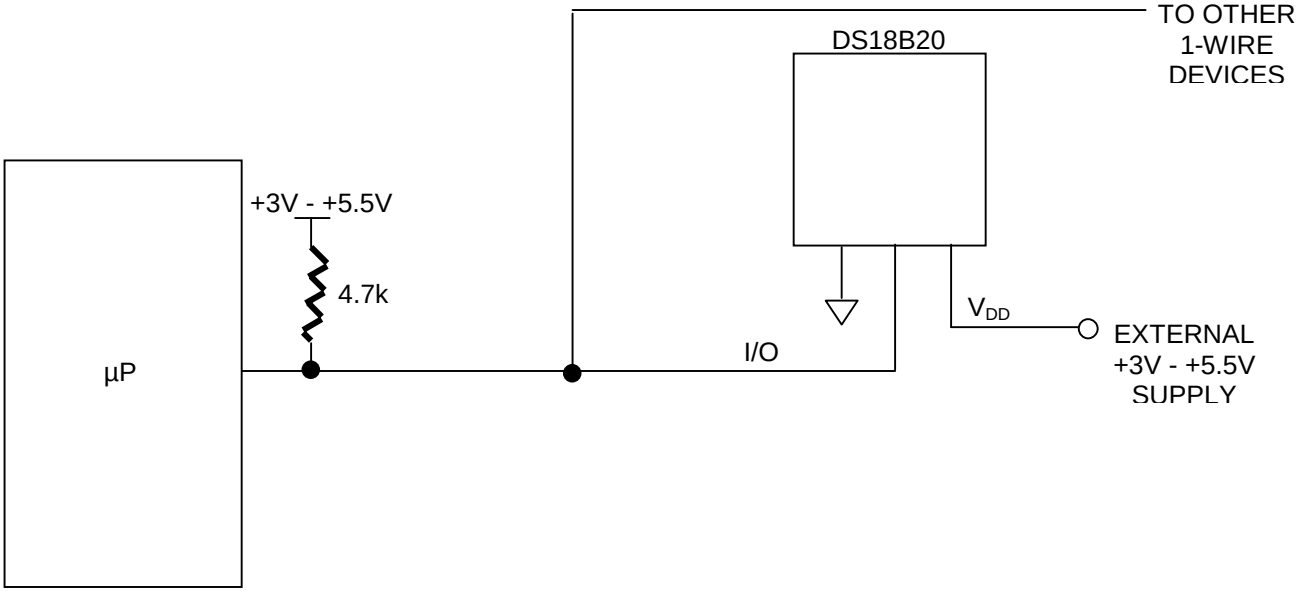
The use of parasite power is not recommended above 100°C, since it may not be able to sustain communications given the higher leakage currents the DS18B20 exhibits at these temperatures. For applications in which such temperatures are likely, it is strongly recommended that V_{DD} be applied to the DS18B20.

For situations where the bus master does not know whether the DS18B20s on the bus are parasite powered or supplied with external V_{DD}, a provision is made in the DS18B20 to signal the power supply scheme used. The bus master can determine if any DS18B20s are on the bus which require the strong pullup by sending a Skip ROM protocol, then issuing the read power supply command. After this command is issued, the master then issues read time slots. The DS18B20 will send back "0" on the 1-Wire bus if it is parasite powered; it will send back a "1" if it is powered from the V_{DD} pin. If the master receives a "0," it knows that it must supply the strong pullup on the DQ line during temperature conversions. See "Memory Command Functions" section for more detail on this command protocol.

STRONG PULLUP FOR SUPPLYING DS18B20 DURING TEMPERATURE CONVERSION Figure 2



USING V_{DD} TO SUPPLY TEMPERATURE CONVERSION CURRENT Figure 3



OPERATION - MEASURING TEMPERATURE

The core functionality of the DS18B20 is its direct-to-digital temperature sensor. The resolution of the DS18B20 is configurable (9, 10, 11, or 12 bits), with 12-bit readings the factory default state. This equates to a temperature resolution of 0.5°C, 0.25°C, 0.125°C, or 0.0625°C. Following the issuance of the Convert T [44h] command, a temperature conversion is performed and the thermal data is stored in the scratchpad memory in a 16-bit, sign-extended two's complement format. The temperature information can be retrieved over the 1-Wire interface by issuing a Read Scratchpad [BEh] command once the conversion has been performed. The data is transferred over the 1-Wire bus, LSB first. The MSB of the temperature register contains the "sign" (S) bit, denoting whether the temperature is positive or negative.

Table 2 describes the exact relationship of output data to measured temperature. The table assumes 12-bit resolution. If the DS18B20 is configured for a lower resolution, insignificant bits will contain zeros. For Fahrenheit usage, a lookup table or conversion routine must be used.

Temperature/Data Relationships Table 2

2^3	2^2	2^1	2^0	2^{-1}	2^{-2}	2^{-3}	2^{-4}	LSB
MSb			(unit = °C)				LSb	
S	S	S	S	S	2^6	2^5	2^4	MSB

TEMPERATURE	DIGITAL OUTPUT (Binary)	DIGITAL OUTPUT (Hex)
+125°C	0000 0111 1101 0000	07D0h
+85°C	0000 0101 0101 0000	0550h*
+25.0625°C	0000 0001 1001 0001	0191h
+10.125°C	0000 0000 1010 0010	00A2h
+0.5°C	0000 0000 0000 1000	0008h
0°C	0000 0000 0000 0000	0000h
-0.5°C	1111 1111 1111 1000	FFF8h
-10.125°C	1111 1111 0101 1110	FF5Eh
-25.0625°C	1111 1110 0110 1111	FF6Fh
-55°C	1111 1100 1001 0000	FC90h

*The power on reset register value is +85°C.

OPERATION - ALARM SIGNALING

After the DS18B20 has performed a temperature conversion, the temperature value is compared to the trigger values stored in TH and TL. Since these registers are 8-bit only, bits 9-12 are ignored for comparison. The most significant bit of TH or TL directly corresponds to the sign bit of the 16-bit temperature register. If the result of a temperature measurement is higher than TH or lower than TL, an alarm flag inside the device is set. This flag is updated with every temperature measurement. As long as the alarm flag is set, the DS18B20 will respond to the alarm search command. This allows many DS18B20s to be connected in parallel doing simultaneous temperature measurements. If somewhere the temperature exceeds the limits, the alarming device(s) can be identified and read immediately without having to read non-alarming devices.

64-BIT LASERED ROM

Each DS18B20 contains a unique ROM code that is 64-bits long. The first 8 bits are a 1-Wire family code (DS18B20 code is 28h). The next 48 bits are a unique serial number. The last 8 bits are a CRC of the first 56 bits. (See Figure 4.) The 64-bit ROM and ROM Function Control section allow the DS18B20 to operate as a 1-Wire device and follow the 1-Wire protocol detailed in the section "1-Wire Bus System." The functions required to control sections of the DS18B20 are not accessible until the ROM function protocol has been satisfied. This protocol is described in the ROM function protocol flowchart (Figure 5). The 1-Wire bus master must first provide one of five ROM function commands: 1) Read ROM, 2) Match ROM, 3) Search ROM, 4) Skip ROM, or 5) Alarm Search. After a ROM function sequence has been successfully executed, the functions specific to the DS18B20 are accessible and the bus master may then provide one of the six memory and control function commands.

CRC GENERATION

The DS18B20 has an 8-bit CRC stored in the most significant byte of the 64-bit ROM. The bus master can compute a CRC value from the first 56-bits of the 64-bit ROM and compare it to the value stored within the DS18B20 to determine if the ROM data has been received error-free by the bus master. The equivalent polynomial function of this CRC is:

$$CRC = X^8 + X^5 + X^4 + 1$$

The DS18B20 also generates an 8-bit CRC value using the same polynomial function shown above and provides this value to the bus master to validate the transfer of data bytes. In each case where a CRC is used for data transfer validation, the bus master must calculate a CRC value using the polynomial function given above and compare the calculated value to either the 8-bit CRC value stored in the 64-bit ROM portion of the DS18B20 (for ROM reads) or the 8-bit CRC value computed within the DS18B20 (which is read as a ninth byte when the scratchpad is read). The comparison of CRC values and decision to continue with an operation are determined entirely by the bus master. There is no circuitry inside the DS18B20 that prevents a command sequence from proceeding if the CRC stored in or calculated by the DS18B20 does not match the value generated by the bus master.

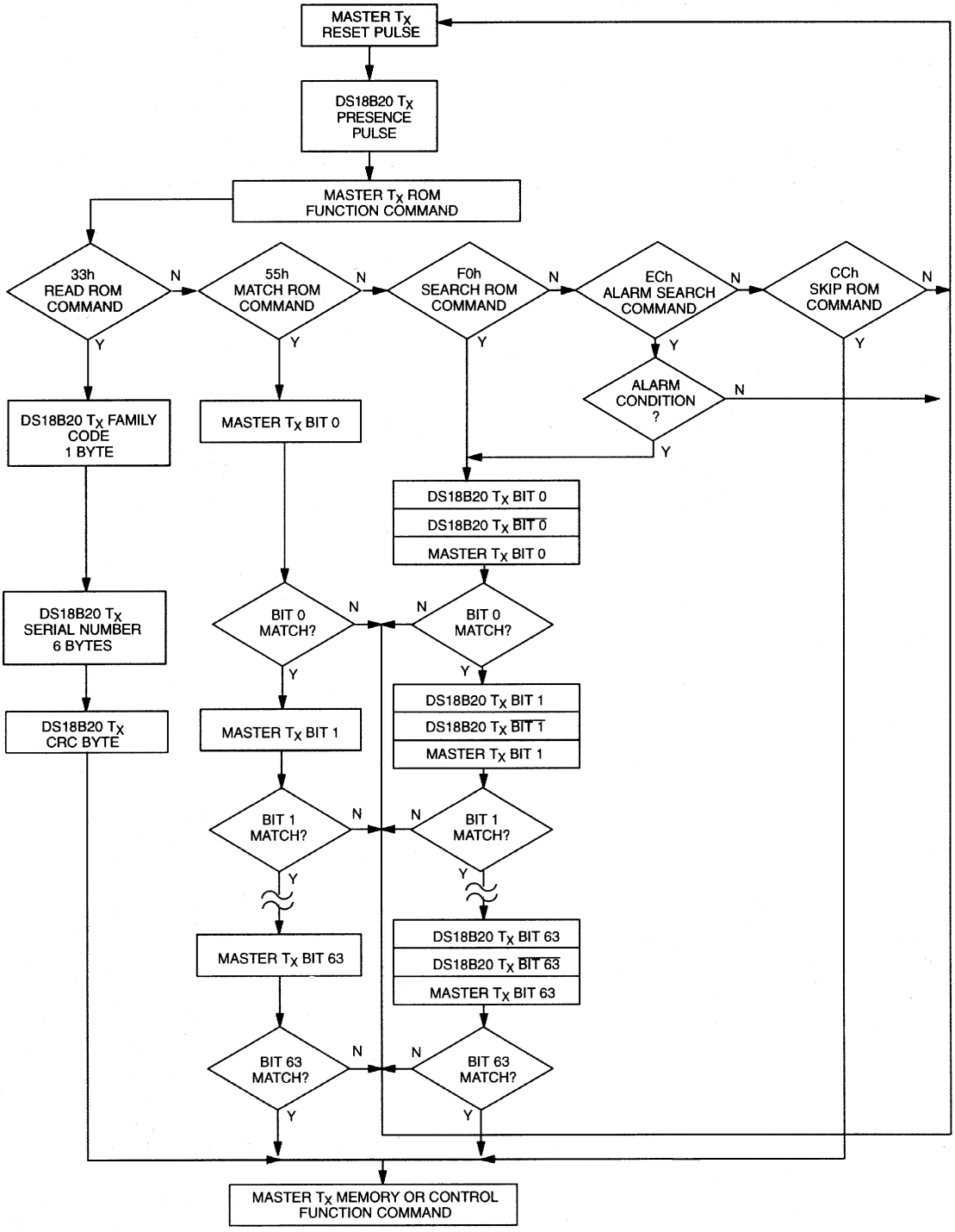
The 1-Wire CRC can be generated using a polynomial generator consisting of a shift register and XOR gates as shown in Figure 6. Additional information about the Dallas 1-Wire Cyclic Redundancy Check is available in Application Note 27 entitled "Understanding and Using Cyclic Redundancy Checks with Dallas Semiconductor Touch Memory Products."

The shift register bits are initialized to 0. Then starting with the least significant bit of the family code, 1 bit at a time is shifted in. After the 8th bit of the family code has been entered, then the serial number is entered. After the 48th bit of the serial number has been entered, the shift register contains the CRC value. Shifting in the 8 bits of CRC should return the shift register to all 0s.

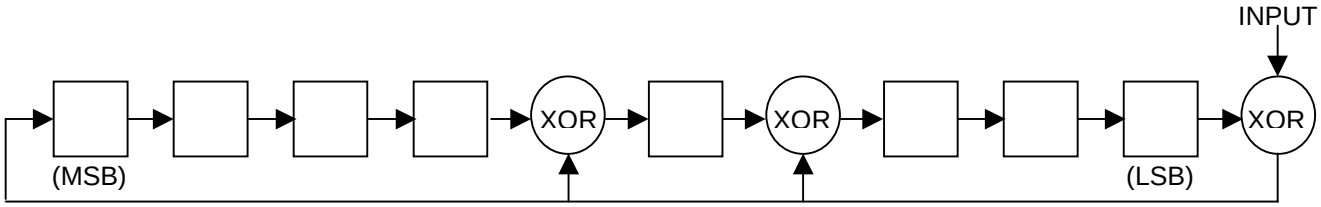
64-BIT LASERED ROM Figure 4

8-BIT CRC CODE		48-BIT SERIAL NUMBER		8-BIT FAMILY CODE (28h)	
MSB	LSB	MSB	LSB	MSB	LSB

ROM FUNCTIONS FLOW CHART Figure 5



1-WIRE CRC CODE Figure 6



MEMORY

The DS18B20's memory is organized as shown in Figure 8. The memory consists of a scratchpad RAM and a nonvolatile, electrically erasable (E^2) RAM, which stores the high and low temperature triggers TH and TL, and the configuration register. The scratchpad helps insure data integrity when communicating over the 1-Wire bus. Data is first written to the scratchpad using the Write Scratchpad [4Eh] command. It can then be verified by using the Read Scratchpad [BEh] command. After the data has been verified, a Copy Scratchpad [48h] command will transfer the data to the nonvolatile (E^2) RAM. This process insures data integrity when modifying memory. The DS18B20 EEPROM is rated for a minimum of 50,000 writes and 10 years data retention at T = +55°C.

The scratchpad is organized as eight bytes of memory. The first 2 bytes contain the LSB and the MSB of the measured temperature information, respectively. The third and fourth bytes are volatile copies of TH and TL and are refreshed with every power-on reset. The fifth byte is a volatile copy of the configuration register and is refreshed with every power-on reset. The configuration register will be explained in more detail later in this section of the datasheet. The sixth, seventh, and eighth bytes are used for internal computations, and thus will not read out any predictable pattern.

It is imperative that one writes TH, TL, and config in succession; i.e. a write is not valid if one writes only to TH and TL, for example, and then issues a reset. If any of these bytes must be written, all three must be written before a reset is issued.

There is a ninth byte which may be read with a Read Scratchpad [BEh] command. This byte contains a cyclic redundancy check (CRC) byte which is the CRC over all of the eight previous bytes. This CRC is implemented in the fashion described in the section titled "CRC Generation".

Configuration Register

The fifth byte of the scratchpad memory is the configuration register.

It contains information which will be used by the device to determine the resolution of the temperature to digital conversion. The bits are organized as shown in Figure 7.

DS18B20 CONFIGURATION REGISTER Figure 7

0	R1	R0	1	1	1	1	1

MSb LSb

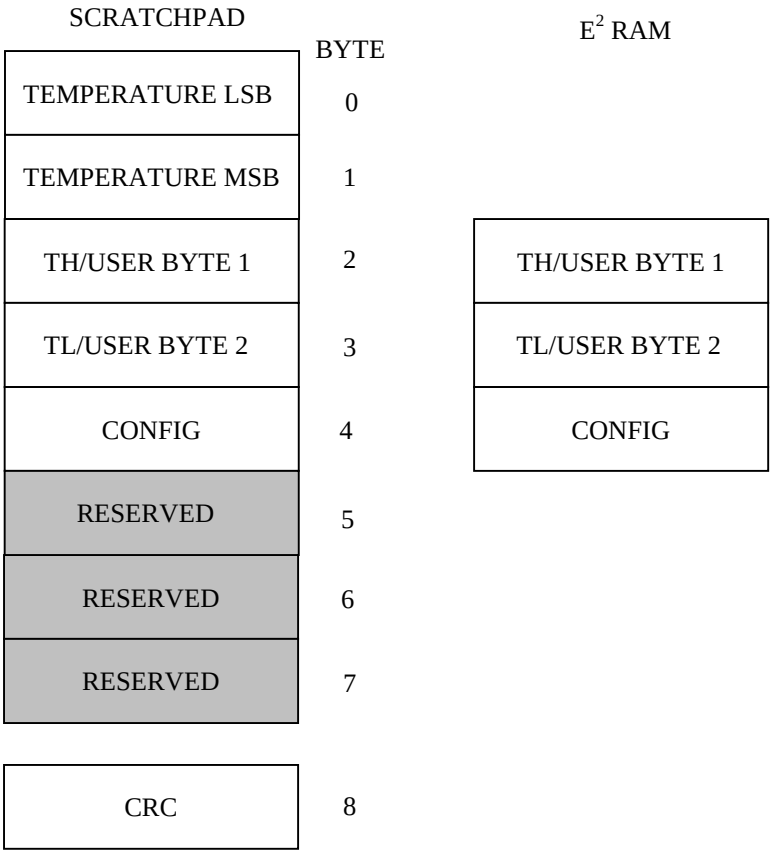
Bits 0-4 are don't cares on a write but will always read out "1".
Bit 7 is a don't care on a write but will always read out "0".

R0, R1: Thermometer resolution bits. Table 3 below defines the resolution of the digital thermometer, based on the settings of these 2 bits. There is a direct tradeoff between resolution and conversion time, as depicted in the AC Electrical Characteristics. The factory default of these EEPROM bits is R0=1 and R1=1 (12-bit conversions).

Thermometer Resolution Configuration Table 3

R1	R0	Thermometer Resolution	Max Conversion Time	
0	0	9 bit	93.75 ms	(t_{conv}/8)
0	1	10 bit	187.5 ms	(t_{conv}/4)
1	0	11 bit	375 ms	(t_{conv}/2)
1	1	12 bit	750 ms	(t_{conv})

DS18B20 MEMORY MAP Figure 8



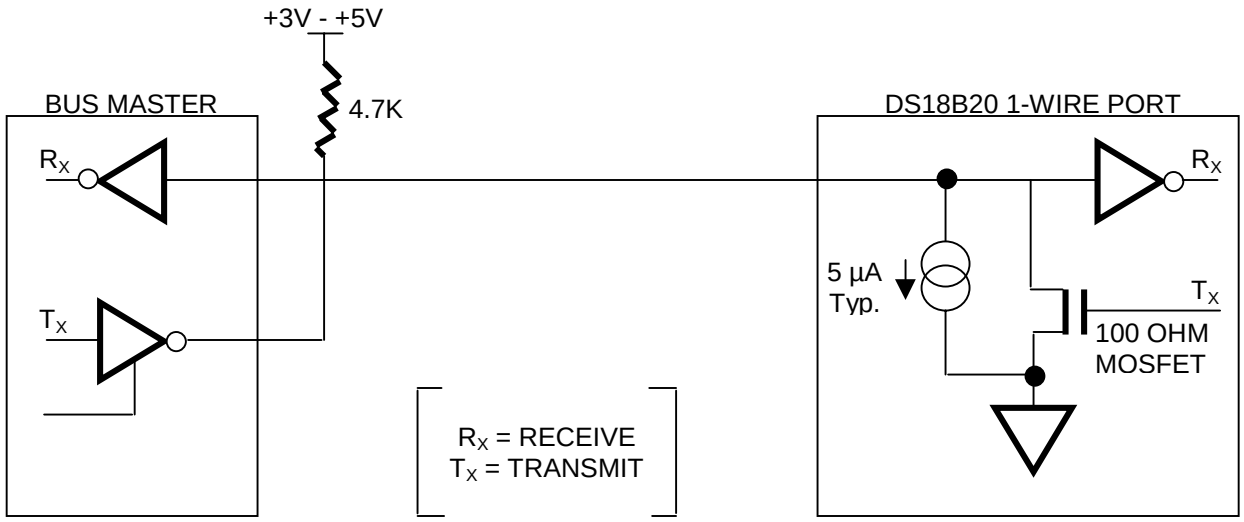
1-WIRE BUS SYSTEM

The 1-Wire bus is a system which has a single bus master and one or more slaves. The DS18B20 behaves as a slave. The discussion of this bus system is broken down into three topics: hardware configuration, transaction sequence, and 1-Wire signaling (signal types and timing).

HARDWARE CONFIGURATION

The 1-Wire bus has only a single line by definition; it is important that each device on the bus be able to drive it at the appropriate time. To facilitate this, each device attached to the 1-Wire bus must have open drain or 3-state outputs. The 1-Wire port of the DS18B20 (DQ pin) is open drain with an internal circuit equivalent to that shown in Figure 9. A multidrop bus consists of a 1-Wire bus with multiple slaves attached. The 1-Wire bus requires a pullup resistor of approximately 5 kΩ.

HARDWARE CONFIGURATION Figure 9



The idle state for the 1-Wire bus is high. If for any reason a transaction needs to be suspended, the bus MUST be left in the idle state if the transaction is to resume. Infinite recovery time can occur between bits so long as the 1-Wire bus is in the inactive (high) state during the recovery period. If this does not occur and the bus is left low for more than 480 µs, all components on the bus will be reset.

TRANSACTION SEQUENCE

The protocol for accessing the DS18B20 via the 1-Wire port is as follows:

- Initialization
- ROM Function Command
- Memory Function Command
- Transaction/Data

INITIALIZATION

All transactions on the 1-Wire bus begin with an initialization sequence. The initialization sequence consists of a reset pulse transmitted by the bus master followed by presence pulse(s) transmitted by the slave(s).

The presence pulse lets the bus master know that the DS18B20 is on the bus and is ready to operate. For more details, see the "1-Wire Signaling" section.

ROM FUNCTION COMMANDS

Once the bus master has detected a presence, it can issue one of the five ROM function commands. All ROM function commands are 8 bits long. A list of these commands follows (refer to flowchart in Figure 5):

Read ROM [33h]

This command allows the bus master to read the DS18B20's 8-bit family code, unique 48-bit serial number, and 8-bit CRC. This command can only be used if there is a single DS18B20 on the bus. If more than one slave is present on the bus, a data collision will occur when all slaves try to transmit at the same time (open drain will produce a wired AND result).

Match ROM [55h]

The match ROM command, followed by a 64-bit ROM sequence, allows the bus master to address a specific DS18B20 on a multidrop bus. Only the DS18B20 that exactly matches the 64-bit ROM sequence will respond to the following memory function command. All slaves that do not match the 64-bit ROM sequence will wait for a reset pulse. This command can be used with a single or multiple devices on the bus.

Skip ROM [CCh]

This command can save time in a single drop bus system by allowing the bus master to access the memory functions without providing the 64-bit ROM code. If more than one slave is present on the bus and a Read command is issued following the Skip ROM command, data collision will occur on the bus as multiple slaves transmit simultaneously (open drain pulldowns will produce a wired AND result).

Search ROM [F0h]

When a system is initially brought up, the bus master might not know the number of devices on the 1-Wire bus or their 64-bit ROM codes. The search ROM command allows the bus master to use a process of elimination to identify the 64-bit ROM codes of all slave devices on the bus.

Alarm Search [ECh]

The flowchart of this command is identical to the Search ROM command. However, the DS18B20 will respond to this command only if an alarm condition has been encountered at the last temperature measurement. An alarm condition is defined as a temperature higher than TH or lower than TL. The alarm condition remains set as long as the DS18B20 is powered up, or until another temperature measurement reveals a non-alarming value. For alarming, the trigger values stored in EEPROM are taken into account. If an alarm condition exists and the TH or TL settings are changed, another temperature conversion should be done to validate any alarm conditions.

Example of a ROM Search

The ROM search process is the repetition of a simple three-step routine: read a bit, read the complement of the bit, then write the desired value of that bit. The bus master performs this simple, three-step routine on each bit of the ROM. After one complete pass, the bus master knows the contents of the ROM in one device. The remaining number of devices and their ROM codes may be identified by additional passes.

The following example of the ROM search process assumes four different devices are connected to the same 1-Wire bus. The ROM data of the four devices is as shown:

ROM1	00110101...
ROM2	10101010...
ROM3	11110101...
ROM4	00010001...

The search process is as follows:

1. The bus master begins the initialization sequence by issuing a reset pulse. The slave devices respond by issuing simultaneous presence pulses.

2. The bus master will then issue the Search ROM command on the 1-Wire bus.

3. The bus master reads a bit from the 1-Wire bus. Each device will respond by placing the value of the first bit of their respective ROM data onto the 1-Wire bus. ROM1 and ROM4 will place a 0 onto the 1-Wire bus, i.e., pull it low. ROM2 and ROM3 will place a 1 onto the 1-Wire bus by allowing the line to stay high. The result is the logical AND of all devices on the line, therefore the bus master sees a 0. The bus master reads another bit. Since the Search ROM data command is being executed, all of the devices on the 1-Wire bus respond to this second read by placing the complement of the first bit of their respective ROM data onto the 1-Wire bus. ROM1 and ROM4 will place a 1 onto the 1-Wire, allowing the line to stay high. ROM2 and ROM3 will place a 0 onto the 1-Wire, thus it will be pulled low. The bus master again observes a 0 for the complement of the first ROM data bit. The bus master has determined that there are some devices on the 1-Wire bus that have a 0 in the first position and others that have a 1.

   The data obtained from the two reads of the three-step routine have the following interpretations:

00	There are still devices attached which have conflicting bits in this position.
01	All devices still coupled have a 0-bit in this bit position.
10	All devices still coupled have a 1-bit in this bit position.
11	There are no devices attached to the 1-Wire bus.

4. The bus master writes a 0. This deselects ROM2 and ROM3 for the remainder of this search pass, leaving only ROM1 and ROM4 connected to the 1-Wire bus.

5. The bus master performs two more reads and receives a 0-bit followed by a 1-bit. This indicates that all devices still coupled to the bus have 0s as their second ROM data bit.

6. The bus master then writes a 0 to keep both ROM1 and ROM4 coupled.

7. The bus master executes two reads and receives two 0-bits. This indicates that both 1-bits and 0-bits exist as the 3rd bit of the ROM data of the attached devices.

8. The bus master writes a 0-bit. This deselects ROM1, leaving ROM4 as the only device still connected.

9. The bus master reads the remainder of the ROM bits for ROM4 and continues to access the part if desired. This completes the first pass and uniquely identifies one part on the 1-Wire bus.

10. The bus master starts a new ROM search sequence by repeating steps 1 through 7.

11. The bus master writes a 1-bit. This decouples ROM4, leaving only ROM1 still coupled.

12. The bus master reads the remainder of the ROM bits for ROM1 and communicates to the underlying logic if desired. This completes the second ROM search pass, in which another of the ROMs was found.

13. The bus master starts a new ROM search by repeating steps 1 through 3.

14. The bus master writes a 1-bit. This deselects ROM1 and ROM4 for the remainder of this search pass, leaving only ROM2 and ROM3 coupled to the system.

15. The bus master executes two Read time slots and receives two 0s.

16. The bus master writes a 0-bit. This decouples ROM3 leaving only ROM2.

17. The bus master reads the remainder of the ROM bits for ROM2 and communicates to the underlying logic if desired. This completes the third ROM search pass, in which another of the ROMs was found.

18. The bus master starts a new ROM search by repeating steps 13 through 15.

19. The bus master writes a 1-bit. This decouples ROM2, leaving only ROM3.

20. The bus master reads the remainder of the ROM bits for ROM3 and communicates to the underlying logic if desired. This completes the fourth ROM search pass, in which another of the ROMs was found.

NOTE:

The bus master learns the unique ID number (ROM data pattern) of one 1-Wire device on each ROM Search operation. The time required to derive the part's unique ROM code is:

$$960\ \mu s + (8 + 3 \times 64)\ 61\ \mu s = 13.16\ ms$$

The bus master is therefore capable of identifying 75 different 1-Wire devices per second.

I/O SIGNALING

The DS18B20 requires strict protocols to insure data integrity. The protocol consists of several types of signaling on one line: reset pulse, presence pulse, write 0, write 1, read 0, and read 1. All of these signals, with the exception of the presence pulse, are initiated by the bus master.

The initialization sequence required to begin any communication with the DS18B20 is shown in Figure 11. A reset pulse followed by a presence pulse indicates the DS18B20 is ready to send or receive data given the correct ROM command and memory function command.

The bus master transmits (TX) a reset pulse (a low signal for a minimum of 480 μs). The bus master then releases the line and goes into a receive mode (RX). The 1-Wire bus is pulled to a high state via the 5k pullup resistor. After detecting the rising edge on the DQ pin, the DS18B20 waits 15-60 μs and then transmits the presence pulse (a low signal for 60-240 μs).

MEMORY COMMAND FUNCTIONS

The following command protocols are summarized in Table 4, and by the flowchart of Figure 10.

Write Scratchpad [4Eh]

This command writes to the scratchpad of the DS18B20, starting at the TH register. The next 3 bytes written will be saved in scratchpad memory at address locations 2 through 4. All 3 bytes must be written before a reset is issued.

Read Scratchpad [BEh]

This command reads the contents of the scratchpad. Reading will commence at byte 0 and will continue through the scratchpad until the ninth (byte 8, CRC) byte is read. If not all locations are to be read, the master may issue a reset to terminate reading at any time.

Copy Scratchpad [48h]

This command copies the scratchpad into the E^2 memory of the DS18B20, storing the temperature trigger bytes in nonvolatile memory. If the bus master issues read time slots following this command, the DS18B20 will output 0 on the bus as long as it is busy copying the scratchpad to E^2; it will return a 1 when the copy process is complete. If parasite-powered, the bus master has to enable a strong pullup for at least 10 ms immediately after issuing this command. The DS18B20 EEPROM is rated for a minimum of 50,000 writes and 10 years data retention at T=+55°C.

Convert T [44h]

This command begins a temperature conversion. No further data is required. The temperature conversion will be performed and then the DS18B20 will remain idle. If the bus master issues read time slots following this command, the DS18B20 will output 0 on the bus as long as it is busy making a temperature conversion; it will return a 1 when the temperature conversion is complete. If parasite-powered, the bus master has to enable a strong pullup for a period greater than t_{conv} immediately after issuing this command.

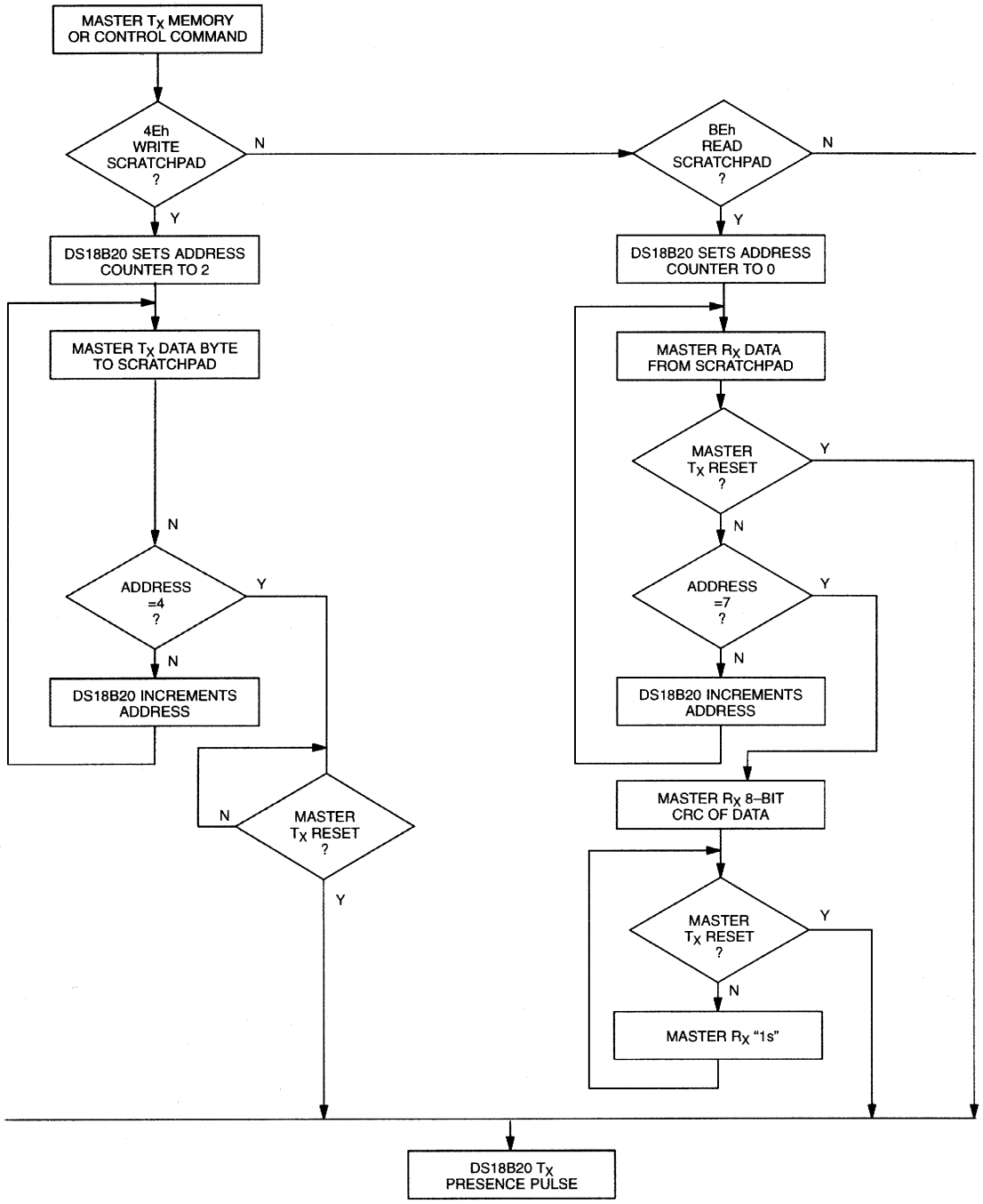
Recall E2 [B8h]

This command recalls the temperature trigger values and configuration register stored in E^2 to the scratchpad. This recall operation happens automatically upon power-up to the DS18B20 as well, so valid data is available in the scratchpad as soon as the device has power applied. With every read data time slot issued after this command has been sent, the device will output its temperature converter busy flag: 0=busy, 1=ready.

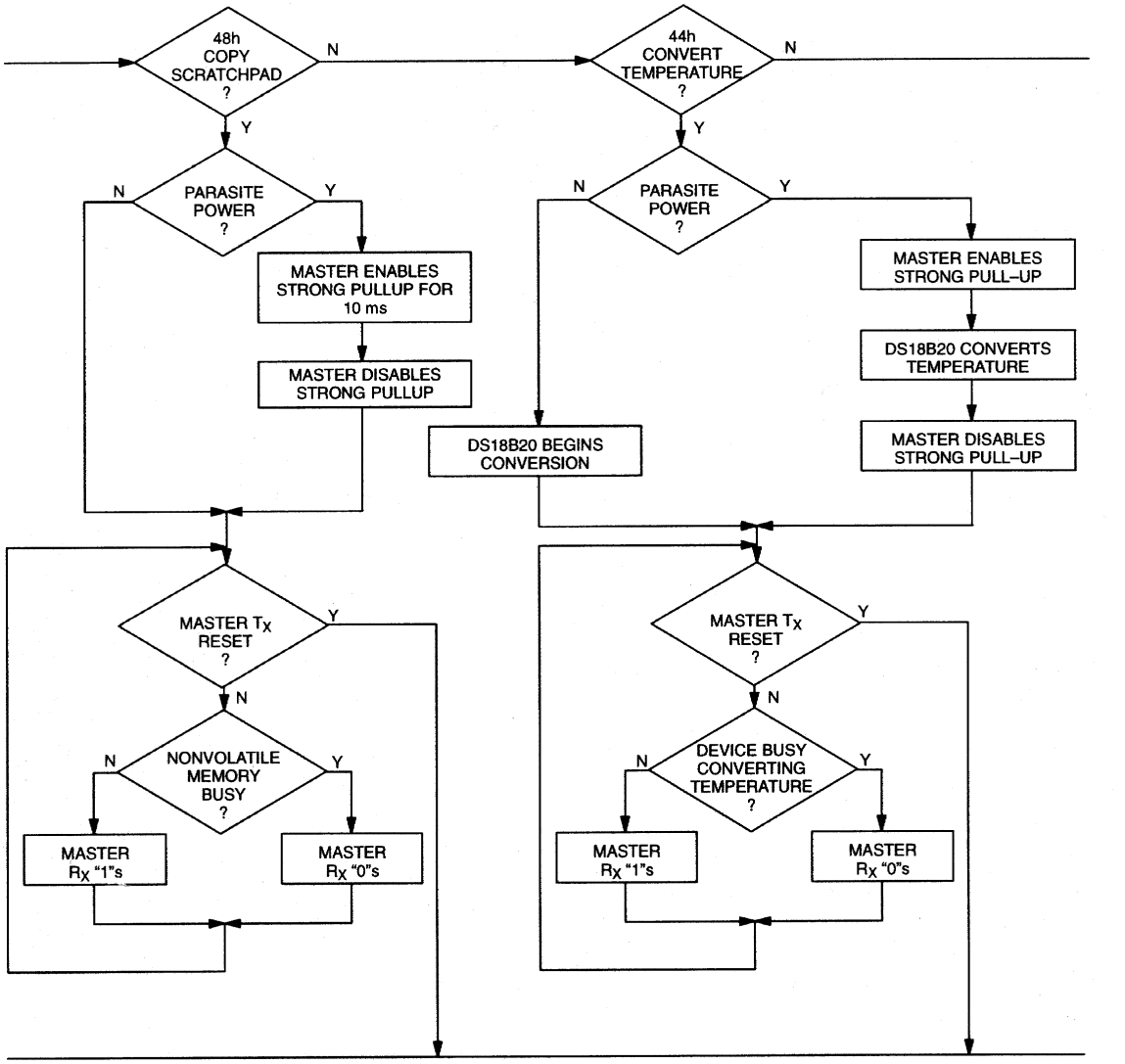
Read Power Supply [B4h]

With every read data time slot issued after this command has been sent to the DS18B20, the device will signal its power mode: 0=parasite power, 1=external power supply provided.

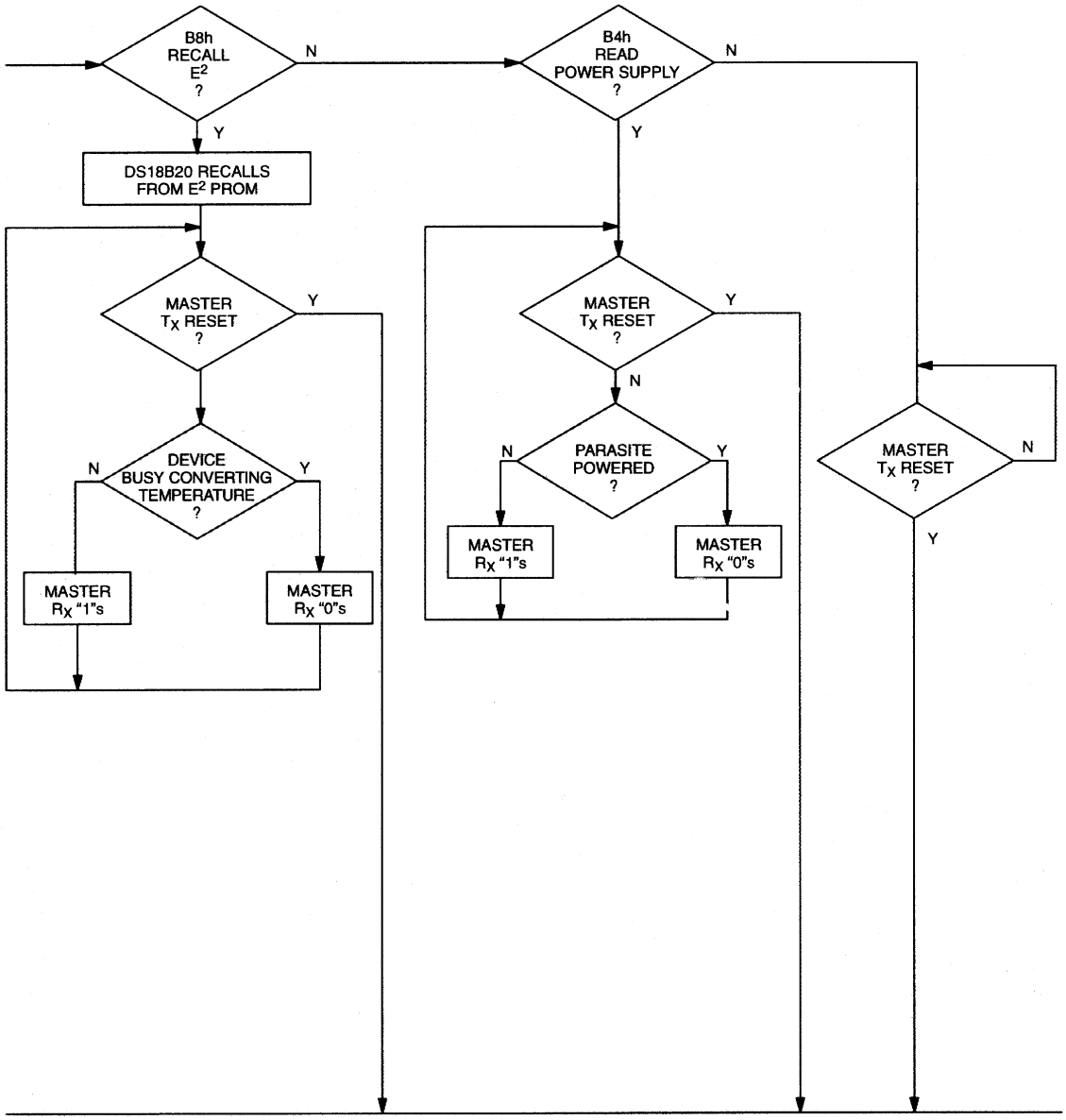
MEMORY FUNCTIONS FLOW CHART Figure 10



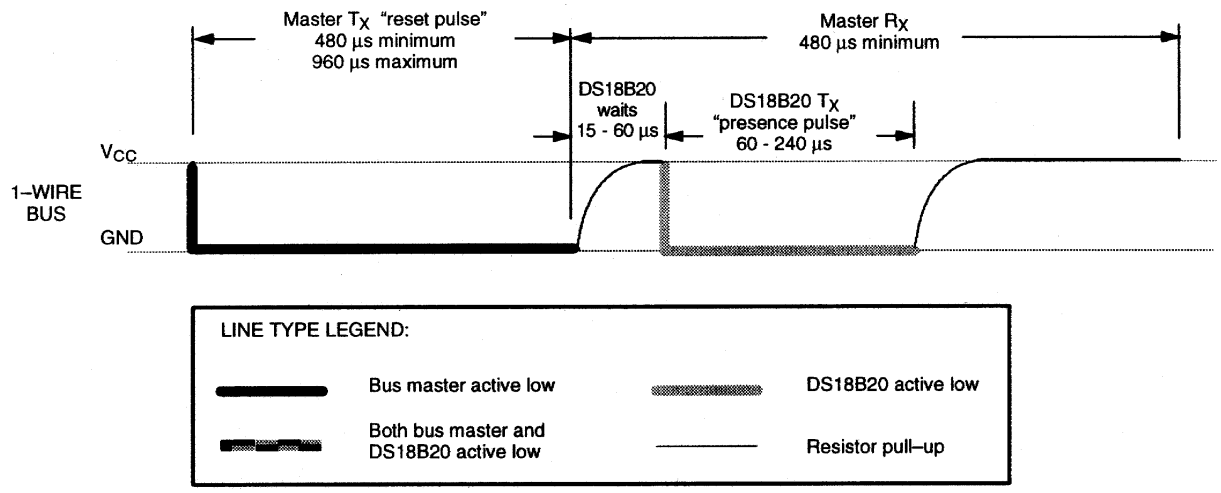
MEMORY FUNCTIONS FLOW CHART Figure 10 (cont'd)



MEMORY FUNCTIONS FLOW CHART Figure 10 (cont'd)



INITIALIZATION PROCEDURE "RESET AND PRESENCE PULSES" Figure 11



DS18B20 COMMAND SET Table 4

INSTRUCTION	DESCRIPTION	PROTOCOL	1-WIRE BUS AFTER ISSUING PROTOCOL	NOTES
TEMPERATURE CONVERSION COMMANDS				
Convert T	Initiates temperature conversion.	44h	<read temperature busy status>	1
MEMORY COMMANDS				
Read Scratchpad	Reads bytes from scratchpad and reads CRC byte.	BEh	<read data up to 9 bytes>	
Write Scratchpad	Writes bytes into scratchpad at addresses 2 through 4 (TH and TL temperature triggers and config).	4Eh	<write data into 3 bytes at addr. 2 through. 4>	3
Copy Scratchpad	Copies scratchpad into nonvolatile memory (addresses 2 through 4 only).	48h	<read copy status>	2
Recall E^2	Recalls values stored in nonvolatile memory into scratchpad (temperature triggers).	B8h	<read temperature busy status>	
Read Power Supply	Signals the mode of DS18B20 power supply to the master.	B4h	<read supply status>	

NOTES:

1. Temperature conversion takes up to 750 ms. After receiving the Convert T protocol, if the part does not receive power from the V_{DD} pin, the DQ line for the DS18B20 must be held high for at least a period greater than t_{conv} to provide power during the conversion process. As such, no other activity may take place on the 1-Wire bus for at least this period after a Convert T command has been issued.

2. After receiving the Copy Scratchpad protocol, if the part does not receive power from the V_{DD} pin, the DQ line for the DS18B20 must be held high for at least 10 ms to provide power during the copy process. As such, no other activity may take place on the 1-Wire bus for at least this period after a Copy Scratchpad command has been issued.

3. All 3 bytes must be written before a reset is issued.

READ/WRITE TIME SLOTS

DS18B20 data is read and written through the use of time slots to manipulate bits and a command word to specify the transaction.

Write Time Slots

A write time slot is initiated when the host pulls the data line from a high logic level to a low logic level. There are two types of write time slots: Write 1 time slots and Write 0 time slots. All write time slots must be a minimum of 60 µs in duration with a minimum of a 1-µs recovery time between individual write cycles.

The DS18B20 samples the DQ line in a window of 15 µs to 60 µs after the DQ line falls. If the line is high, a Write 1 occurs. If the line is low, a Write 0 occurs (see Figure 12).

For the host to generate a Write 1 time slot, the data line must be pulled to a logic low level and then released, allowing the data line to pull up to a high level within 15 µs after the start of the write time slot.

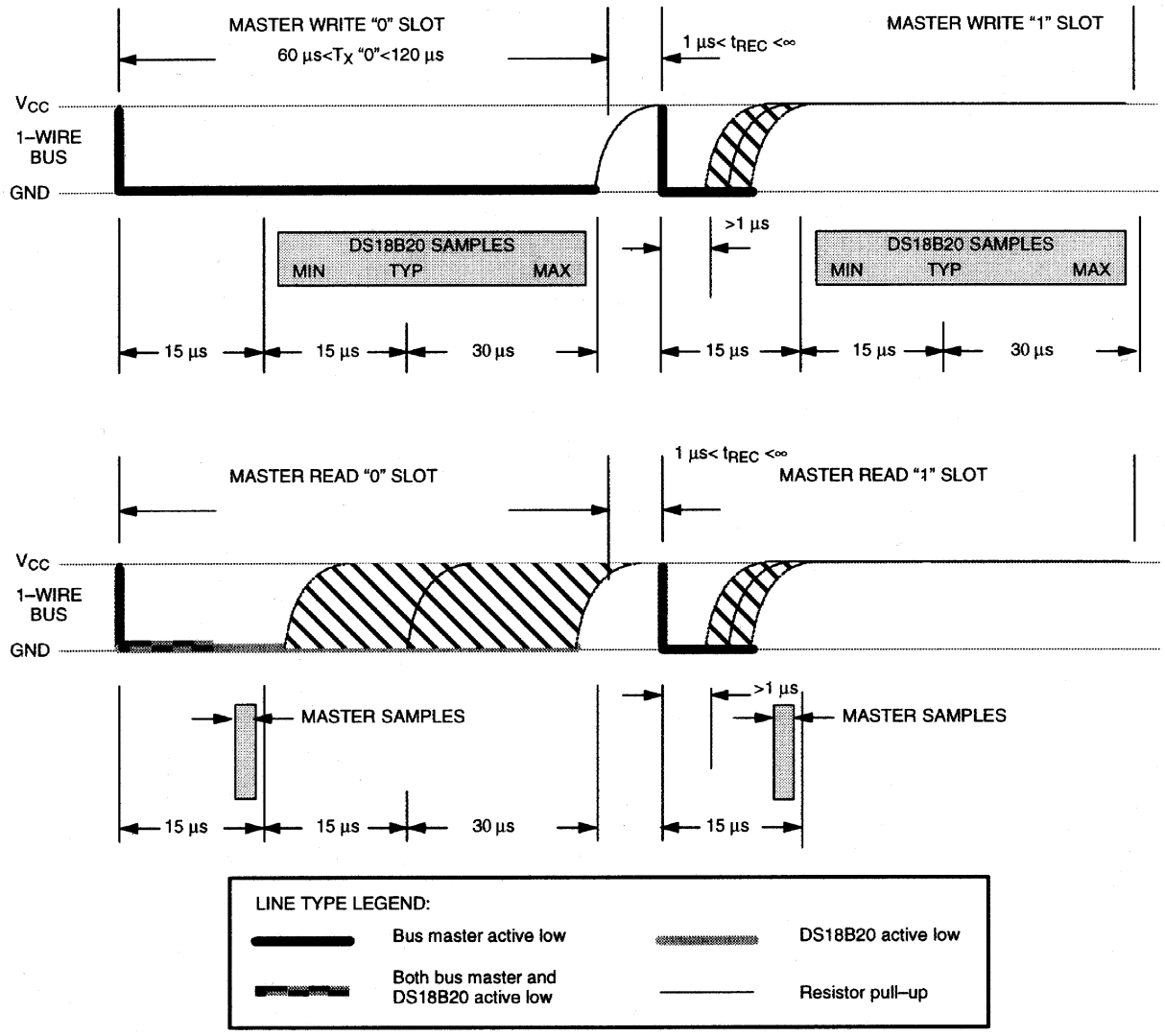
For the host to generate a Write 0 time slot, the data line must be pulled to a logic low level and remain low for 60 µs.

Read Time Slots

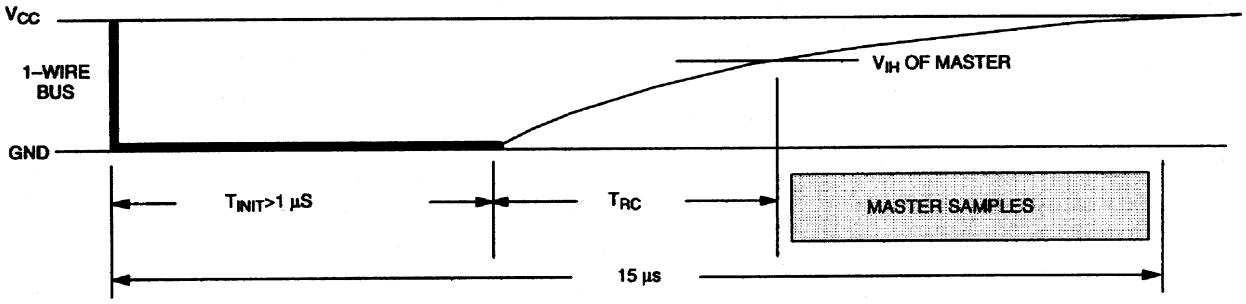
The host generates read time slots when data is to be read from the DS18B20. A read time slot is initiated when the host pulls the data line from a logic high level to logic low level. The data line must remain at a low logic level for a minimum of 1 µs; output data from the DS18B20 is valid for 15 µs after the falling edge of the read time slot. The host therefore must stop driving the DQ pin low in order to read its state 15 µs from the start of the read slot (see Figure 12). By the end of the read time slot, the DQ pin will pull back high via the external pullup resistor. All read time slots must be a minimum of 60 µs in duration with a minimum of a 1-µs recovery time between individual read slots.

Figure 12 shows that the sum of T_{INIT}, T_{RC}, and T_{SAMPLE} must be less than 15 µs. Figure 14 shows that system timing margin is maximized by keeping T_{INIT} and T_{RC} as small as possible and by locating the master sample time towards the end of the 15-µs period.

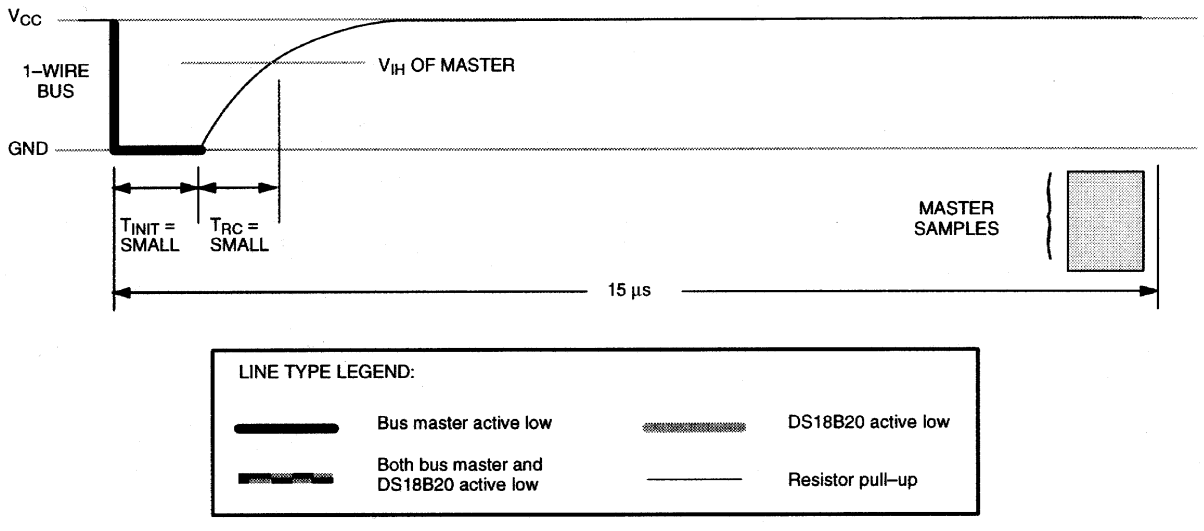
READ/WRITE TIMING DIAGRAM Figure 12



DETAILED MASTER READ 1 TIMING Figure 13



RECOMMENDED MASTER READ 1 TIMING Figure 14



Related Application Notes

The following Application Notes can be applied to the DS18B20. These notes can be obtained from the Dallas Semiconductor "Application Note Book," via our website at http://www.dalsemi.com/.

Application Note 27: "Understanding and Using Cyclic Redundancy Checks with Dallas Semiconductor Touch Memory Product"

Application Note 55: "Extending the Contact Range of Touch Memories"

Application Note 74: "Reading and Writing Touch Memories via Serial Interfaces"

Application Note 104: "Minimalist Temperature Control Demo"

Application Note 106: "Complex MicroLANs"

Application Note 108: "MicroLAN - In the Long Run"

Sample 1-Wire subroutines that can be used in conjunction with AN74 can be downloaded from the website or our Anonymous FTP Site.

MEMORY FUNCTION EXAMPLE Table 5

Example: Bus Master initiates temperature conversion, then reads temperature (parasite power assumed).

MASTER MODE	DATA (LSB FIRST)	COMMENTS
TX	Reset	Reset pulse (480-960 µs).
RX	Presence	Presence pulse.
TX	55h	Issue "Match ROM" command.
TX	<64-bit ROM code>	Issue address for DS18B20.
TX	44h	Issue " Convert T" command.
TX	<I/O LINE HIGH>	I/O line is held high for at least a period of time greater than t_{conv} by bus master to allow conversion to complete.
TX	Reset	Reset pulse.
RX	Presence	Presence pulse.
TX	55h	Issue "Match ROM" command.
TX	<64-bit ROM code>	Issue address for DS18B20.
TX	BEh	Issue "Read Scratchpad" command.
RX	<9 data bytes>	Read entire scratchpad plus CRC; the master now recalculates the CRC of the eight data bytes received from the scratchpad, compares the CRC calculated and the CRC read. If they match, the master continues; if not, this read operation is repeated.
TX	Reset	Reset pulse.
RX	Presence	Presence pulse, done.

MEMORY FUNCTION EXAMPLE Table 6

Example: Bus Master writes memory (parasite power and only one DS18B20 assumed).

MASTER MODE	DATA (LSB FIRST)	COMMENTS
TX	Reset	Reset pulse.
RX	Presence	Presence pulse.
TX	CCh	Skip ROM command.
TX	4Eh	Write Scratchpad command.
TX	<3 data bytes>	Writes three bytes to scratchpad (TH, TL, and config).
TX	Reset	Reset pulse.
RX	Presence	Presence pulse.
TX	CCh	Skip ROM command.
TX	BEh	Read Scratchpad command.
RX	<9 data bytes>	Read entire scratchpad plus CRC. The master now recalculates the CRC of the eight data bytes received from the scratchpad, compares the CRC and the two other bytes read back from the scratchpad. If data match, the master continues; if not, repeat the sequence.
TX	Reset	Reset pulse.
RX	Presence	Presence pulse.
TX	CCh	Skip ROM command.
TX	48h	Copy Scratchpad command; after issuing this command, the master must wait 10 ms for copy operation to complete.
TX	Reset	Reset pulse.
RX	Presence	Presence pulse, done.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	-0.5V to +6.0V
Operating Temperature	-55°C to +125°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	See J-STD-020A specification

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{DD}	Local Power	3.0		5.5	V	1
Data Pin	DQ		-0.3		+5.5	V	1
Logic 1	V_{IH}		2.2		V_{CC}+ 0.3	V	1,2
Logic 0	V_{IL}		-0.3		+0.8	V	1,3,7

DC ELECTRICAL CHARACTERISTICS (-55°C to +125°C; V_{DD}=3.0V to 5.5V)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS	NOTES
Thermometer Error	t_{ERR}	-10°C to +85°C			±½	°C	
		-55°C to +125°C			±2		
Input Logic High	V_{IH}	Local Power Parasite Power	2.2 3.0		5.5	V V	1,2 1,2
Input Logic Low	V_{IL}		-0.3		+0.8	V	1,3,7
Sink Current	I_L	$V_{I/O}$=0.4V	-4.0			mA	1
Standby Current	I_{DDS}			750	1000	nA	6,8
Active Current	I_{DD}			1	1.5	mA	4
DQ-Input Load Current	I_{DQ}			5		µA	5

AC ELECTRICAL CHARACTERISTICS: NV MEMORY

(-55°C to +125°C; V_{DD}=3.0V to 5.5V)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS	NOTES
NV Write Cycle Time	t_{wr}			2	10	ms	
EEPROM Writes	N_{EEWR}	-55°C to +55°C	50k			writes	
EEPROM Data Retention	t_{EEDR}	-55°C to +55°C	10			years	

AC ELECTRICAL CHARACTERISTICS: (-55°C to +125°C; V_{DD}=3.0V to 5.5V)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS	NOTES
Temperature Conversion Time	t_{CONV}	9 bit			93.75	ms	
		10 bit			187.5		
		11 bit			375		
		12 bit			750		
Time Slot	t_{SLOT}		60		120	µs	
Recovery Time	t_{REC}		1			µs	
Write 0 Low Time	r_{LOW0}		60		120	µs	
Write 1 Low Time	t_{LOW1}		1		15	µs	
Read Data Valid	t_{RDV}				15	µs	
Reset Time High	t_{RSTH}		480			µs	
Reset Time Low	t_{RSTL}		480			µs	9
Presence Detect High	t_{PDHIGH}		15		60	µs	
Presence Detect Low	t_{PDLOW}		60		240	µs	
Capacitance	$C_{IN/OUT}$				25	pF	

NOTES:

1. All voltages are referenced to ground.

2. Logic one voltages are specified at a source current of 1 mA.

3. Logic zero voltages are specified at a sink current of 4 mA.

4. Active current refers to either temperature conversion or writing to the E^2 memory. Writing to E^2 memory consumes approximately 200 µA for up to 10 ms.

5. Input load is to ground.

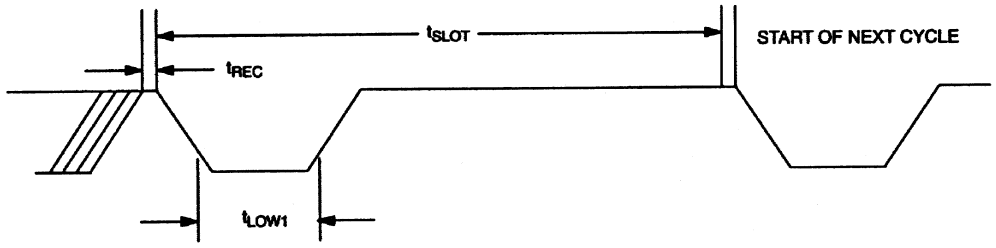
6. Standby current specified up to 70°C. Standby current typically is 3 µA at 125°C.

7. To always guarantee a presence pulse under low voltage parasite power conditions, V_{ILMAX} may have to be reduced to as much as 0.5V.

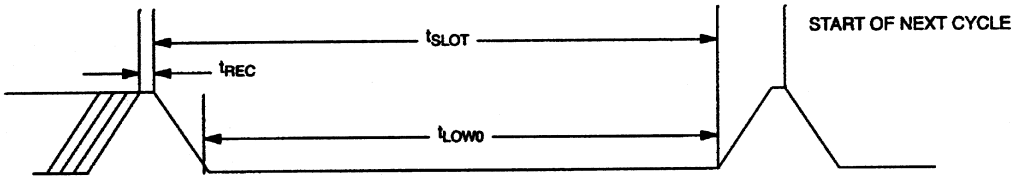
8. To minimize I_{DDS}, DQ should be: GND ≤ DQ ≤ GND +0.3V or V_{DD} – 0.3V ≤ DQ ≤ V_{DD}.

9. Under parasite power, the max t_{RSTL} before a power on reset occurs is 960 µS.

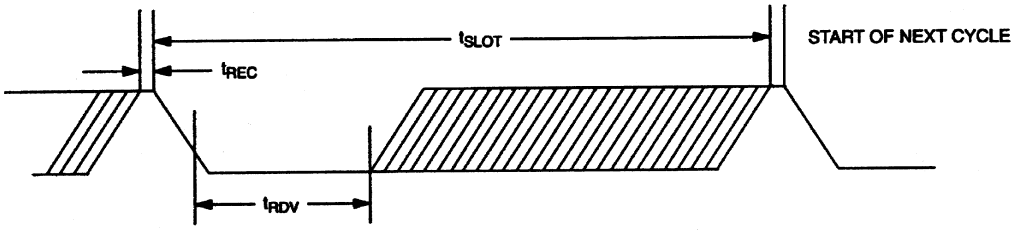
1–WIRE WRITE ONE TIME SLOT



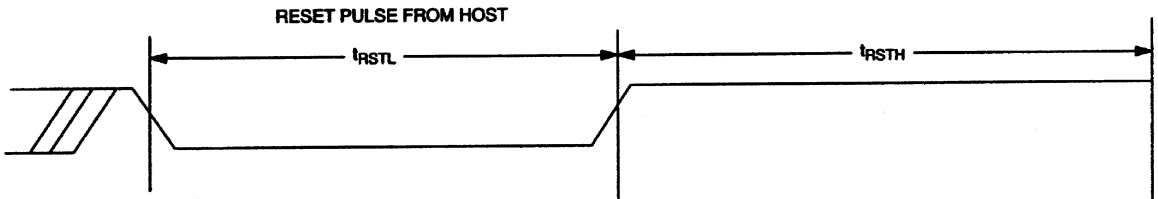
1–WIRE WRITE ZERO TIME SLOT



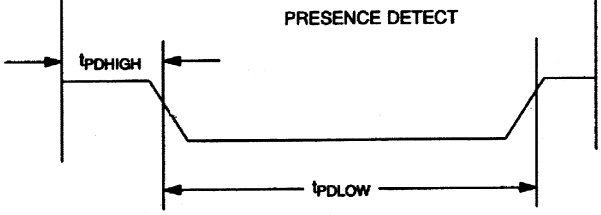
1–WIRE READ ZERO TIME SLOT



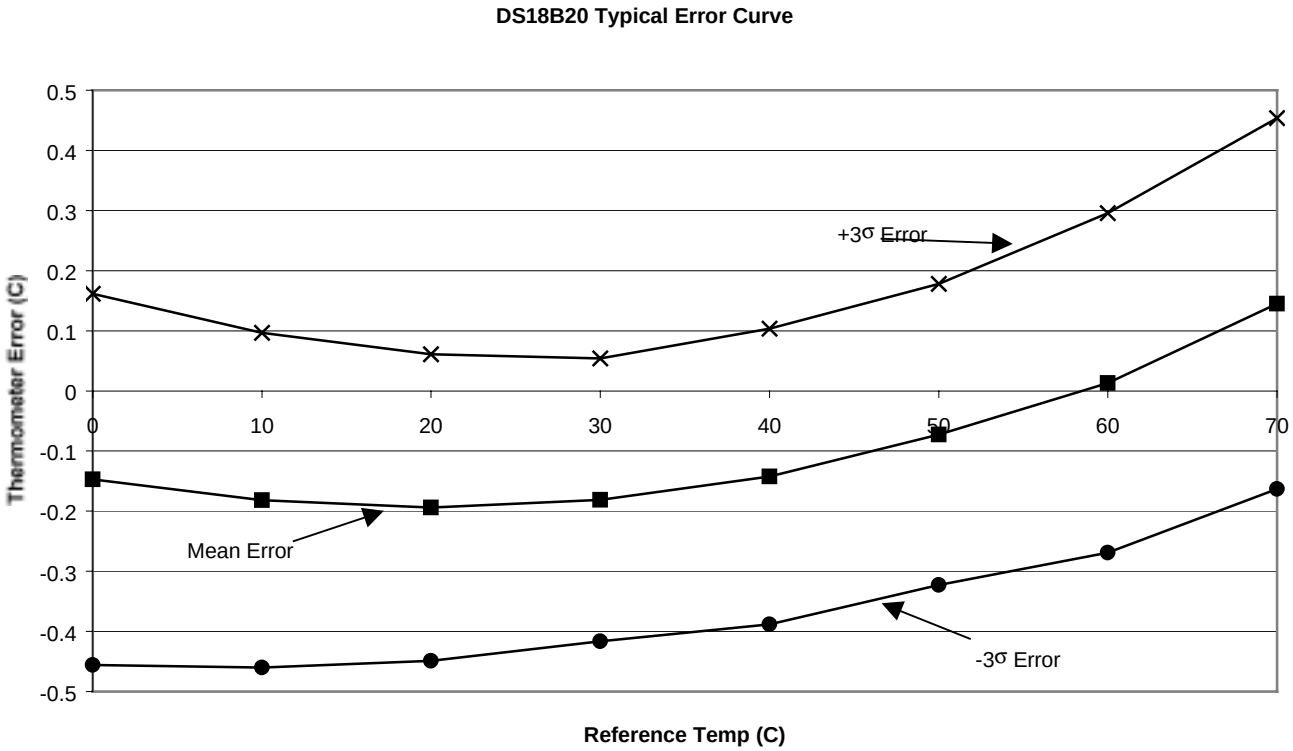
1–WIRE RESET PULSE



1–WIRE PRESENCE DETECT



TYPICAL PERFORMANCE CURVE



MAX30100

Pulse Oximeter and Heart-Rate Sensor IC for Wearable Health

General Description

The MAX30100 is an integrated pulse oximetry and heart-rate monitor sensor solution. It combines two LEDs, a photodetector, optimized optics, and low-noise analog signal processing to detect pulse oximetry and heart-rate signals.

The MAX30100 operates from 1.8V and 3.3V power supplies and can be powered down through software with negligible standby current, permitting the power supply to remain connected at all times.

Applications

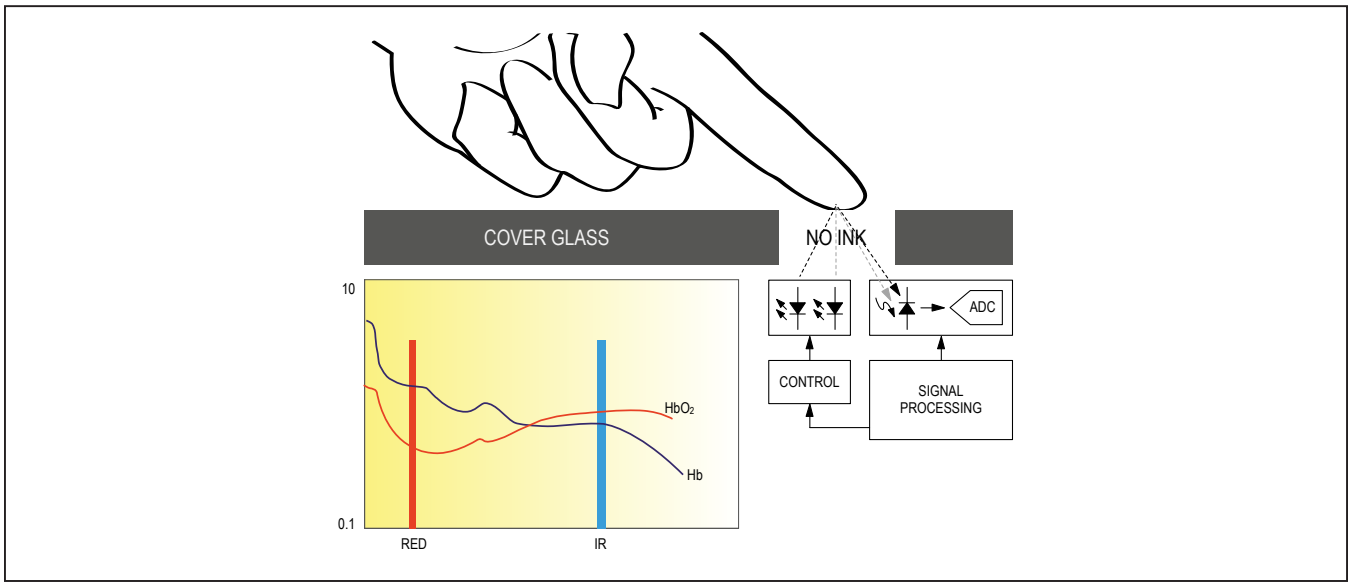
- Wearable Devices
- Fitness Assistant Devices
- Medical Monitoring Devices

Benefits and Features

- Complete Pulse Oximeter and Heart-Rate Sensor Solution Simplifies Design
  - Integrated LEDs, Photo Sensor, and High-Performance Analog Front -End
  - Tiny 5.6mm x 2.8mm x 1.2mm 14-Pin Optically Enhanced System-in-Package
- Ultra-Low-Power Operation Increases Battery Life for Wearable Devices
  - Programmable Sample Rate and LED Current for Power Savings
  - Ultra-Low Shutdown Current (0.7µA, typ)
- Advanced Functionality Improves Measurement Performance
  - High SNR Provides Robust Motion Artifact Resilience
  - Integrated Ambient Light Cancellation
  - High Sample Rate Capability
  - Fast Data Output Capability

***Ordering Information* appears at end of data sheet.**

System Block Diagram



19-7065; Rev 0; 9/14

maxim integrated™

Absolute Maximum Ratings

V_{DD} to GND .....-0.3V to +2.2V
GND to PGND .....-0.3V to +0.3V
x_DRV, x_LED+ to PGND .....-0.3V to +6.0V
All Other Pins to GND .....-0.3V to +6.0V
Output Short-Circuit Current Duration .....Continuous
Continuous Input Current into Any Terminal .....±20mA

Continuous Power Dissipation (T_A = +70°C)
OESIP (derate 5.8mW/°C above +70°C) 464mW
Operating Temperature Range ..... -40°C to +85°C
Soldering Temperature (reflow) .....+260°C
Storage Temperature Range ..... -40°C to +105°C

Package Thermal Characteristics (Note 1)

OESIP
Junction-to-Ambient Thermal Resistance (θ_{JA}) .....150°C/W
Junction-to-Case Thermal Resistance (θ_{JC}) .....170°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(V_{DD} = 1.8V, V_{IR_LED+} = V_{R_LED+} = 3.3V, T_A = +25°C, min/max are from T_A = -40°C to +85°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
POWER SUPPLY							
Power-Supply Voltage	V_{DD}	Guaranteed by RED and IR count tolerance		1.7	1.8	2.0	V
LED Supply Voltage (R_LED+ or IR_LED+ to PGND)	V_{LED+}	Guaranteed by PSRR of LED Driver		3.1	3.3	5.0	V
Supply Current	I_{DD}	SpO_2 and heart rate modes, PW = 200µs, 50sps			600	1200	µA
		Heart rate only mode, PW = 200µs, 50sps			600	1200	
Supply Current in Shutdown	I_{SHDN}	T_A = +25°C, MODE = 0x80			0.7	10	µA
SENSOR CHARACTERISTICS							
ADC Resolution					14		bits
Red ADC Count (Note 3)	RED_C	Propriety ATE setup RED_PA = 0x05, LED_PW = 0x00, SPO2_SR = 0x07, T_A = +25°C		23,000	26,000	29,000	Counts
IR ADC Count (Note 3)	IR_C	Propriety ATE setup IR_PA = 0x09, LED_PW = 0x00, SPO2_SR = 0x07, T_A = +25°C		23,000	26,000	29,000	Counts
Dark Current Count	DC_C	RED_PA = IR_PA = 0x00, LED_PW = 0x03, SPO2_SR = 0x01			0	3	Counts
DC Ambient Light Rejection (Note 4)	ALR	Number of ADC counts with finger on sensor under direct sunlight (100K lux) LED_PW = 0x03, SPO2_SR = 0x01	RED LED		0		Counts
			IR LED		0		

Electrical Characteristics (continued)

(V_{DD} = 1.8V, V_{IR_LED+} = V_{R_LED+} = 3.3V, T_A = +25°C, min/max are from T_A = -40°C to +85°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
IR ADC Count—PSRR (V_{DD})	$PSRR_{VDD}$	Propriety ATE setup 1.7V < V_{DD} < 2.0V, LED_PW = 0x03, SPO2_SR = 0x01, IR_PA = 0x09, IR_PA = 0x05, T_A = +25°C		0.25	2	%
		Frequency = DC to 100kHz, 100mV_{P-P}		10		LSB
RED/IR ADC Count—PSRR (X_LED+)	$PSRR_{LED}$	Propriety ATE setup 3.1V < X_LED+ < 5V, LED_PW = 0x03, SPO2_SR = 0x01, IR_PA = 0x09, IR_PA = 0x05, T_A = +25°C		0.05	2	%
		Frequency = DC to 100kHz, 100mV_{P-P}		10		LSB
ADC Integration Time	INT	LED_PW = 0x00		200		µs
		LED_PW = 0x03		1600		µs
IR LED CHARACTERISTICS (Note 4)						
LED Peak Wavelength	λ_P	I_{LED} = 20mA, T_A = +25°C	870	880	900	nm
Full Width at Half Max	$\Delta\lambda$	I_{LED} = 20mA, T_A = +25°C		30		nm
Forward Voltage	V_F	I_{LED} = 20mA, T_A = +25°C		1.4		V
Radiant Power	P_O	I_{LED} = 20mA, T_A = +25°C		6.5		mW
RED LED CHARACTERISTICS (Note 4)						
LED Peak Wavelength	λ_P	I_{LED} = 20mA, T_A = +25°C	650	660	670	nm
Full Width at Half Max	$\Delta\lambda$	I_{LED} = 20mA, T_A = +25°C		20		nm
Forward Voltage	V_F	I_{LED} = 20mA, T_A = +25°C		2.1		V
Radiant Power	P_O	I_{LED} = 20mA, T_A = +25°C		9.8		mW
TEMPERATURE SENSOR						
Temperature ADC Acquisition Time	T_T	T_A = +25°C		29		ms
Temperature Sensor Accuracy	T_A	T_A = +25°C		±1		°C
Temperature Sensor Minimum Range	T_{MIN}			-40		°C
Temperature Sensor Maximum Range	T_{MAX}			85		°C

Electrical Characteristics (continued)

(V_{DD} = 1.8V, V_{IR_LED+} = V_{R_LED+} = 3.3V, T_A = +25°C, min/max are from T_A = -40°C to +85°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL CHARACTERISTICS (SDA, SDA, $\overline{INT}$)						
Output Low Voltage SDA, $\overline{INT}$	V_{OL}	I_{SINK} = 6mA			0.4	V
I²C Input Voltage Low	V_{IL_I2C}	SDA, SCL			0.4	V
I²C Input Voltage High	V_{IH_I2C}	SDA, SCL	1.4			V
Input Hysteresis	V_{HYS}	SDA, SCL		200		mV
Input Capacitance	C_{IN}	SDA, SCL		10		pF
Input Leakage Current	I_{IN}	V_{IN} = 0V, T_A = +25°C (SDA, SCL, INT)		0.01	1	µA
		V_{IN} = 5.5V, T_A = +25°C (SDA, SCL, INT)		0.01	1	µA
I²C TIMING CHARACTERISTICS (SDA, SDA, $\overline{INT}$)						
I²C Write Address				AE		Hex
I²C Read Address				AF		Hex
Serial Clock Frequency	f_{SCL}		0		400	kHz
Bus Free Time Between STOP and START Conditions	t_{BUF}		1.3			µs
Hold Time (Repeated) START Condition	$t_{HD,START}$		0.6			µs
SCL Pulse-Width Low	t_{LOW}		1.3			µs
SCL Pulse-Width High	t_{HIGH}		0.6			µs
Setup Time for a Repeated START Condition	$t_{SU,START}$		0.6			µs
Data Hold Time	$t_{HD,DAT}$		0		900	ns
Data Setup Time	$t_{SU,DAT}$		100			ns
Setup Time for STOP Condition	$t_{SU,STOP}$		0.6			µs
Pulse Width of Suppressed Spike	t_{SP}		0		50	ns
Bus Capacitance	C_B				400	pF
SDA and SCL Receiving Rise Time	t_R		20 + 0.1C_B		300	ns
SDA and SCL Receiving Fall Time	t_{RF}		20 + 0.1C_B		300	ns
SDA Transmitting Fall Time	t_{TF}		20 + 0.1C_B		300	ns

Note 2: All devices are 100% production tested at T_A = +25°C. Specifications over temperature limits are guaranteed by Maxim Integrated's bench or proprietary automated test equipment (ATE) characterization.

Note 3: Specifications are guaranteed by Maxim Integrated's bench characterization and by 100% production test using proprietary ATE setup and conditions.

Note 4: For design guidance only. Not production tested.

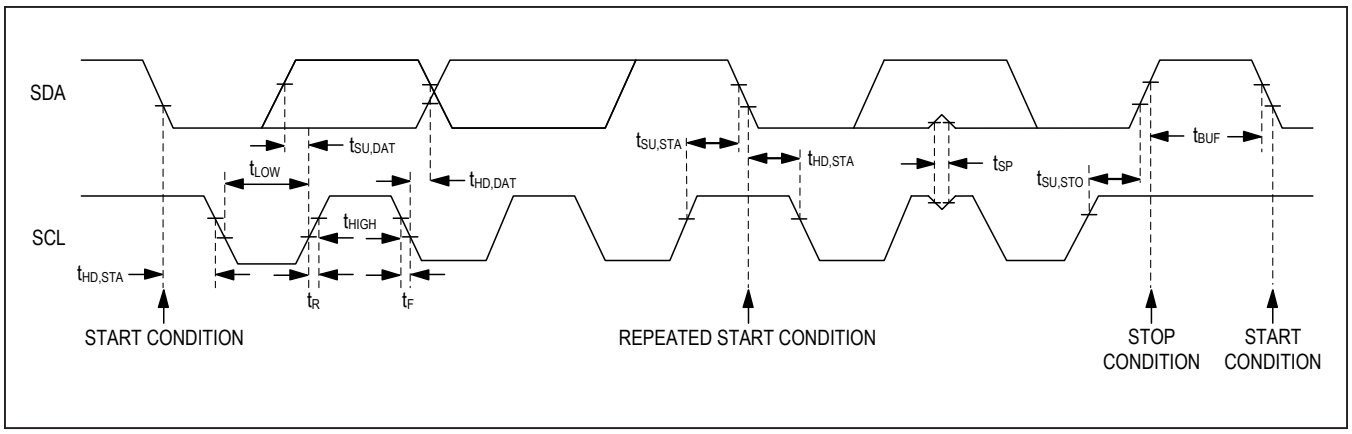
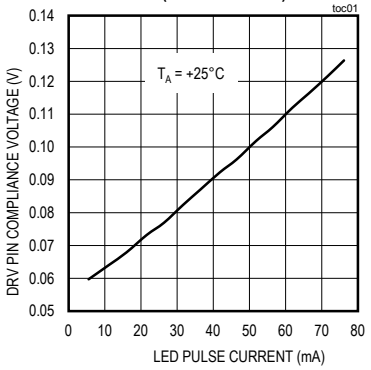


Figure 1. I²C-Compatible Interface Timing Diagram

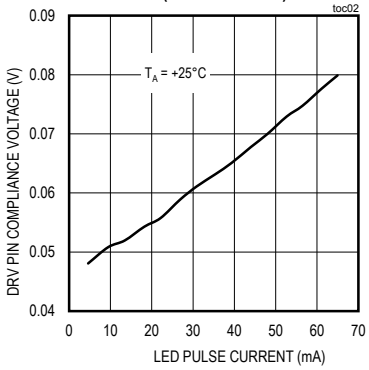
Typical Operating Characteristics

(V_{DD} = 1.8V, V_{IR_LED+} = V_{R_LED+} = 3.3V, T_A = +25°C, unless otherwise noted.)

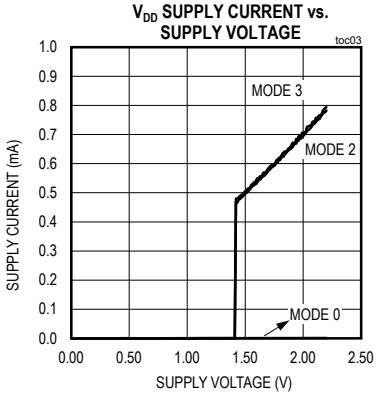
RED LED SUPPLY HEADROOM (-10% CURRENT)



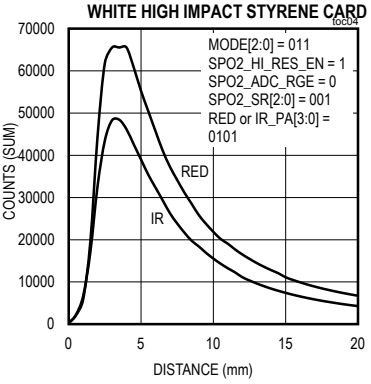
IR LED SUPPLY HEADROOM (-10% CURRENT)



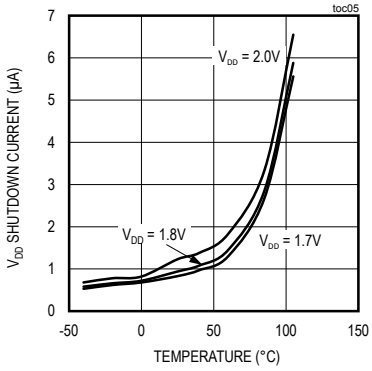
V_{DD} SUPPLY CURRENT vs. SUPPLY VOLTAGE



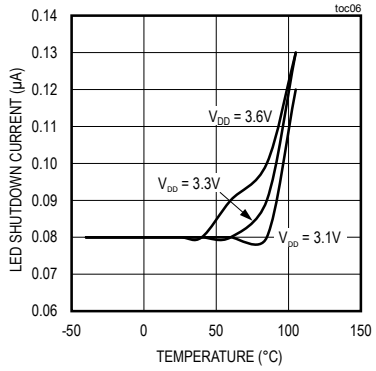
DC COUNTS vs. DISTANCE FOR WHITE HIGH IMPACT STYRENE CARD



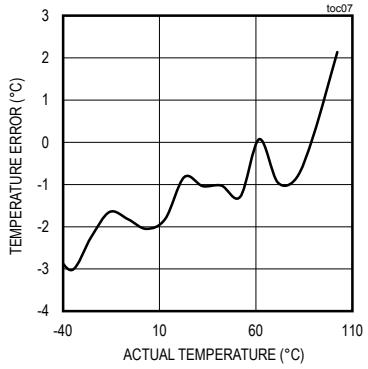
V_{DD} SHUTDOWN CURRENT vs. TEMPERATURE



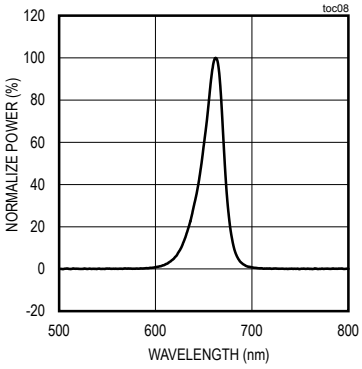
LED SHUTDOWN CURRENT vs. TEMPERATURE



ON-BOARD TEMPERATURE vs. ERROR



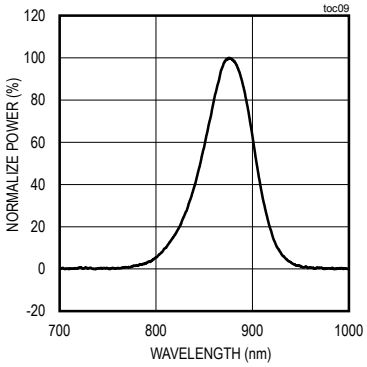
RED LED SPECTRA at +30°C



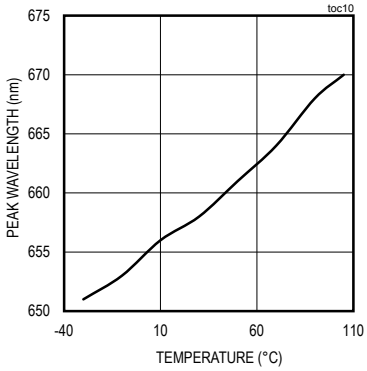
Typical Operating Characteristics (continued)

(V_{DD} = 1.8V, V_{IR_LED+} = V_{R_LED+} = 3.3V, T_A = +25°C, unless otherwise noted.)

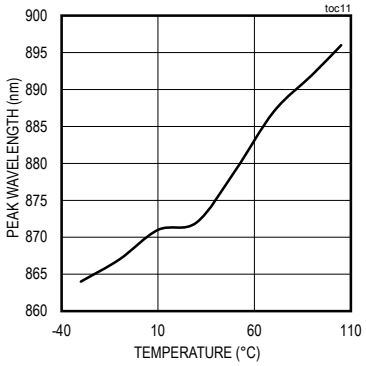
IR LED SPECTRA at +30°C



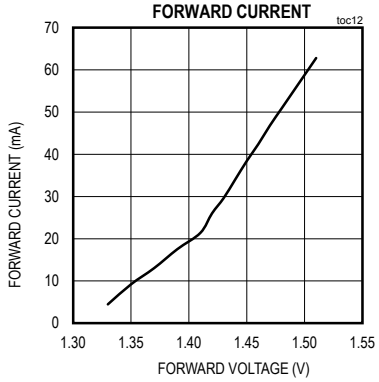
RED LED WAVELENGTH vs. TEMPERATURE AT LED CURRENT = 25mA



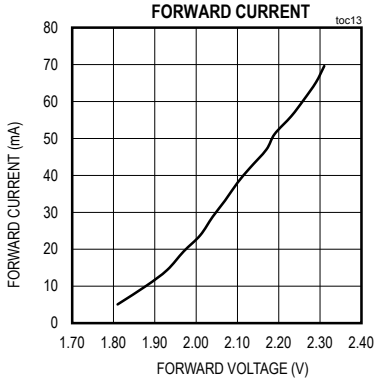
IR LED WAVELENGTH vs. TEMPERATURE AT LED CURRENT = 25mA



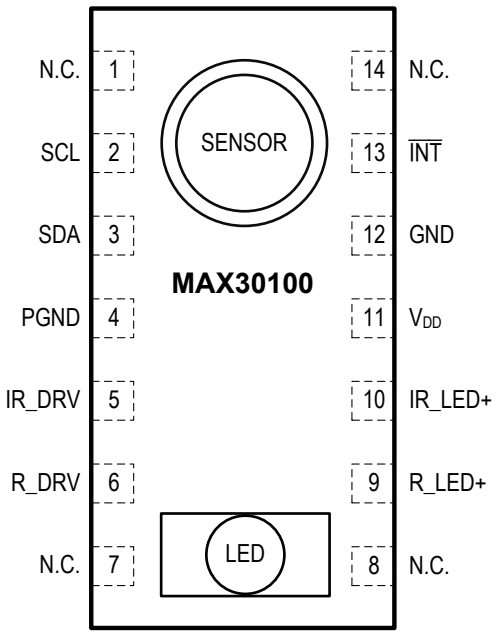
RED LED FORWARD VOLTAGE vs. FORWARD CURRENT



IR LED FORWARD VOLTAGE vs. FORWARD CURRENT



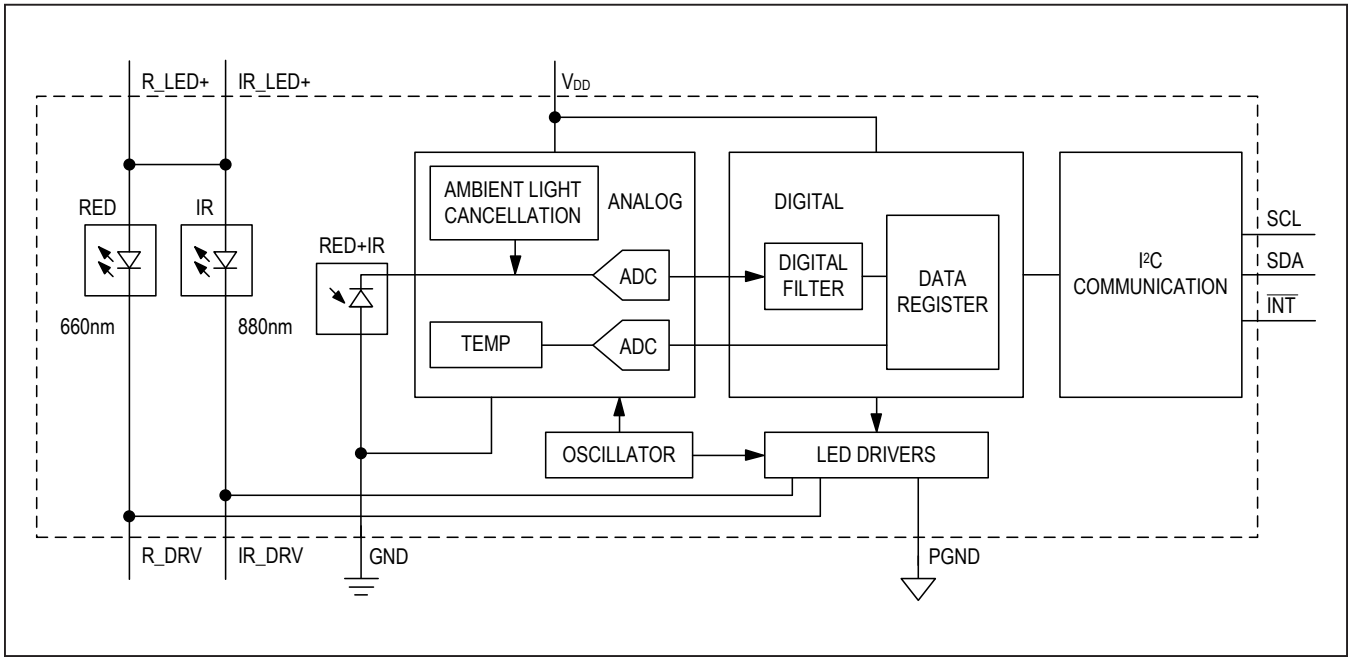
Pin Configuration



Pin Description

PIN	NAME	FUNCTION
1, 7, 8, 14	N.C.	No Connection. Connect to PCB Pad for Mechanical Stability.
2	SCL	I^2C Clock Input
3	SDA	I^2C Clock Data, Bidirectional (Open-Drain)
4	PGND	Power Ground of the LED Driver Blocks
5	IR_DRV	IR LED Cathode and LED Driver Connection Point. Leave floating in circuit.
6	R_DRV	Red LED Cathode and LED Driver Connection Point. Leave floating in circuit.
9	R_LED+	Power Supply (Anode Connection) for Red LED. Bypass to PGND for best performance. Connected to IR_LED+ internally.
10	IR_LED+	Power Supply (Anode Connection) for IR LED. Bypass to PGND for best performance. Connected to R_LED+ internally.
11	V_{DD}	Analog Power Supply Input. Bypass to GND for best performance.
12	GND	Analog Ground
13	$\overline{INT}$	Active-Low Interrupt (Open-Drain)

Functional Diagram



Detailed Description

The MAX30100 is a complete pulse oximetry and heart-rate sensor system solution designed for the demanding requirements of wearable devices. The MAX30100 provides very small total solution size without sacrificing optical or electrical performance. Minimal external hardware components are needed for integration into a wearable device.

The MAX30100 is fully configurable through software registers, and the digital output data is stored in a 16-deep FIFO within the device. The FIFO allows the MAX30100 to be connected to a microcontroller or microprocessor on a shared bus, where the data is not being read continuously from the device's registers.

SpO_2 Subsystem

The SpO_2 subsystem in the MAX30100 is composed of ambient light cancellation (ALC), 16-bit sigma delta ADC, and proprietary discrete time filter.

The SpO_2 ADC is a continuous time oversampling sigma delta converter with up to 16-bit resolution. The ADC output data rate can be programmed from 50Hz to 1kHz. The MAX30100 includes a proprietary discrete time filter to reject 50Hz/60Hz interference and low-frequency residual ambient noise.

Temperature Sensor

The MAX30100 has an on-chip temperature sensor for (optionally) calibrating the temperature dependence of the SpO_2 subsystem.

The SpO_2 algorithm is relatively insensitive to the wavelength of the IR LED, but the red LED's wavelength is critical to correct interpretation of the data. The temperature sensor data can be used to compensate the SpO_2 error with ambient temperature changes.

LED Driver

The MAX30100 integrates red and IR LED drivers to drive LED pulses for SpO_2 and HR measurements. The LED current can be programmed from 0mA to 50mA (typical only) with proper supply voltage. The LED pulse width can be programmed from 200µs to 1.6ms to optimize measurement accuracy and power consumption based on use cases.

Table 1. Register Maps and Descriptions

REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	REG ADDR	POR STATE	R/W
STATUS											
Interrupt Status	A_FULL	TEMP_RDY	HR_RDY	SPO2_RDY				PWR_RDY	0x00	0X00	R
Interrupt Enable	ENB_A_FULL	ENB_TEP_RDY	ENB_HR_RDY	ENB_SO2_RDY					0x01	0X00	R/W
FIFO											
FIFO Write Pointer					FIFO_WR_PTR[3:0]				0x02	0x00	R/W
Over Flow Counter					OVF_COUNTER[3:0]				0x03	0x00	R/W
FIFO Read Pointer					FIFO_RD_PTR[3:0]				0x04	0x00	R/W
FIFO Data Register	FIFO_DATA[7:0]								0x05	0x00	R/W
CONFIGURATION											
Mode Configuration	SHDN	RESET			TEMP_EN	MODE[2:0]			0x06	0x00	R/W
SPO2 Configuration		SPO2_HI_RES_EN	RESERVED	SPO2_SR[2:0]			LED_PW[1:0]		0x07	0x00	R/W
RESERVED									0x08	0x00	R/W
LED Configuration	RED_PA[3:0]				IR_PA[3:0]				0x09	0x00	R/W
RESERVED									0x0A – 0x15	0x00	R/W
TEMPERATURE											
Temp_Integer	TINT[7:0]								0x16	0x00	R/W
Temp_Fraction					TFRAC[3:0]				0x17	0x00	R/W
RESERVED									0x8D	0x00	R/W
PART ID											
Revision ID	REV_ID[7:0]								0xFE	0xXX*	R
Part ID	PART_ID[7]								0xFF	0x11	R/W

*XX denotes any 2-digit hexidecimal number (00 to FF). Contact Maxim Integrated for the Revision ID number assigned for your product.

Interrupt Status (0x00)

REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	REG ADDR	POR STATE	R/W
Interrupt Status	A_FULL	TEMP_ RDY	HR_RDY	SPO2_ RDY				PWR_ RDY	0x00	0X00	R

There are 5 interrupts and the functionality of each is exactly the same: pulling the active-low interrupt pin into its low state until the interrupt is cleared.

The interrupts are cleared whenever the interrupt status register is read, or when the register that triggered the interrupt is read. For example, if the SpO_2 sensor triggers an interrupt due to finishing a conversion, reading either the FIFO data register or the interrupt register clears the interrupt pin (which returns to its normal high state), and also clears all the bits in the interrupt status register to zero.

Bit 7: FIFO Almost Full Flag (A_FULL)

In SpO_2 and heart-rate modes, this interrupt triggers when the FIFO write pointer is the same as the FIFO read pointer minus one, which means that the FIFO has only one unwritten space left. If the FIFO is not read within the next conversion time, the FIFO becomes full and future data is lost.

Bit 6: Temperature Ready Flag (TEMP_RDY)

When an internal die temperature conversion is finished, this interrupt is triggered so the processor can read the temperature data registers.

Bit 5: Heart Rate Data Ready (HR_RDY)

In heart rate or SPO_2 mode, this interrupt triggers after every data sample is collected. A heart rate data sample consists of one IR data point only. This bit is automatically cleared when the FIFO data register is read.

Bit 4: SpO_2 Data Ready (SPO2_RDY)

In SpO_2 mode, this interrupt triggers after every data sample is collected. An SpO_2 data sample consists of one IR and one red data points. This bit is automatically cleared when the FIFO data register is read.

Bit 3: RESERVED

This bit should be ignored and always be zero in normal operation.

Bit 2: RESERVED

This bit should be ignored and always be zero in normal operation.

Bit 1: RESERVED

This bit should be ignored and always be zero in normal operation.

Bit 0: Power Ready Flag (PWR_RDY)

On power-up or after a brownout condition, when the supply voltage V_{DD} transitions from below the UVLO voltage to above the UVLO voltage, a power-ready interrupt is triggered to signal that the IC is powered up and ready to collect data.

Interrupt Enable (0x01)

REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	REG ADDR	POR STATE	R/W
Interrupt Enable	ENB_A_FULL	ENB_TEMP_RDY	ENB_HR_RDY	ENB_SO2_RDY					0x01	0X00	R/W

Each source of hardware interrupt, with the exception of power ready, can be disabled in a software register within the MAX30100 IC. The power-ready interrupt cannot be disabled because the digital state of the MAX30100 is reset upon a brownout condition (low power-supply voltage), and the default state is that all the interrupts are disabled. It is important for the system to know that a brownout condition has occurred, and the data within the device is reset as a result.

When an interrupt enable bit is set to zero, the corresponding interrupt appears as 1 in the interrupt status register, but the $\overline{INT}$ pin is not pulled low.

The four unused bits (B3:B0) should always be set to zero (disabled) for normal operation.

FIFO (0x02–0x05)

REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	REG ADDR	POR STATE	R/W
FIFO Write Pointer					FIFO_WR_PTR[3:0]				0x02	0x00	R/W
Over Flow Counter					OVF_COUNTER[3:0]				0x03	0x00	R/W
FIFO Read Pointer					FIFO_RD_PTR[3:0]				0x04	0x00	R/W
FIFO Data Register	FIFO_DATA[7:0]								0x05	0x00	R/W

FIFO Write Pointer

The FIFO write pointer points to the location where the MAX30100 writes the next sample. This pointer advances for each sample pushed on to the FIFO. It can also be changed through the I^2C interface when MODE[2:0] is nonzero.

FIFO Overflow Counter

When the FIFO is full, samples are not pushed on to the FIFO, samples are lost. OVF_COUNTER counts the number of samples lost. It saturates at 0xF. When a complete sample is popped from the FIFO (when the read pointer advances), OVF_COUNTER is reset to zero.

FIFO Read Pointer

The FIFO read pointer points to the location from where the processor gets the next sample from the FIFO via the I^2C interface. This advances each time a sample is popped from the FIFO. The processor can also write to this pointer after reading the samples, which would allow rereading samples from the FIFO if there is a data communication error.

FIFO Data

The circular FIFO depth is 16 and can hold up to 16 samples of SpO_2 channel data (Red and IR). The FIFO_DATA register in the I^2C register map points to the next sample to be read from the FIFO. FIFO_RD_PTR points to this sample. Reading FIFO_DATA register does not automatically increment the register address; burst reading this register reads the same address over and over. Each sample is 4 bytes of data, so this register has to be read 4 times to get one sample.

The above registers can all be written and read, but in practice, only the FIFO_RD_PTR register should be written to in operation. The others are automatically incremented or filled with data by the MAX30100. When starting a new SpO_2

or heart-rate conversion, it is recommended to first clear the FIFO_WR_PTR, OVF_COUNTER, and FIFO_RD_PTR registers to all zeros (0x00) to ensure the FIFO is empty and in a known state. When reading the MAX30100 registers in one burst-read I2C transaction, the register address pointer typically increments so that the next byte of data sent is from the next register, etc. The exception to this is the FIFO data register, register 0x05. When reading this register, the address pointer does not increment, but the FIFO_RD_PTR does. So the next byte of data sent will represent the next byte of data available in the FIFO.

Reading from the FIFO

Normally, reading registers from the I2C interface autoincrements the register address pointer, so that all the registers can be read in a burst read without an I2C restart event. In the MAX30100, this holds true for all registers except for the FIFO_DATA register (0x05).

Reading the FIFO_DATA register does not automatically increment the register address; burst reading this register reads the same address over and over. Each sample is 4 bytes of data, so this register has to be read 4 times to get one sample.

The other exception is 0xFF, reading more bytes after the 0xFF register does not advance the address pointer back to 0x00, and the data read is not meaningful.

FIFO Data Structure

The data FIFO consists of a 16-sample memory bank that stores both IR and RED ADC data. Since each sample consists of one IR word and one RED word, there are 4 bytes of data for each sample, and therefore, 64 total bytes of data can be stored in the FIFO. Figure 2 shows the structure of the FIFO graphically.

The FIFO data is left-justified as shown in Table 1; i.e. the MSB bit is always in the bit 15 position regardless of ADC resolution.

Each data sample consists of an IR and a red data word (2 registers), so to read one sample requires 4 I2C byte reads in a row. The FIFO read pointer is automatically incremented after each 4-byte sample is read.

In heart-rate only mode, the 3rd and 4th bytes of each sample return zeros, but the basic structure of the FIFO remains the same.

Write/Read Pointers

Table 2. FIFO Data

ADC RESOLUTION	IR [15]	IR [14]	IR [13]	IR [12]	IR [11]	IR [10]	IR [9]	IR [8]	IR [7]	IR [6]	IR [5]	IR [4]	IR [3]	IR [2]	IR [1]	IR [0]
16-bit																
14-bit																
12-bit																
10-bit																

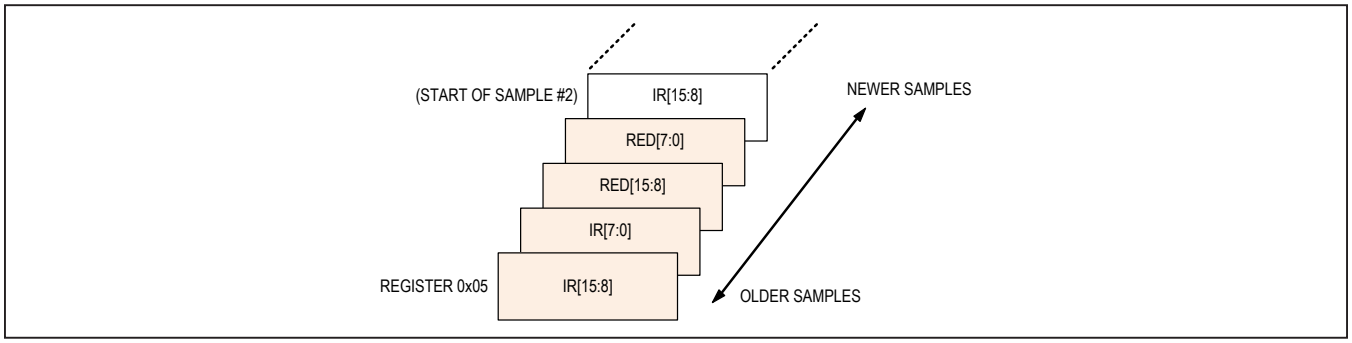


Figure 2. Graphical Representation of the FIFO Data Register

The locations to store new data, and the read pointer for reading data, are used to control the flow of data in the FIFO. The write pointer increments every time a new sample is added to the FIFO. The read pointer is incremented automatically every time a sample is read from the FIFO. To reread a sample from the FIFO, decrement its value by one and read the data register again.

The SpO_2 write/read pointers should be cleared (back to 0x0) upon entering SpO_2 mode or heart-rate mode, so that there is no old data represented in the FIFO. The pointers are not automatically cleared when changing modes, but they are cleared if V_{DD} is power cycled so that the V_{DD} voltage drops below its UVLO voltage.

Pseudo-Code Example of Reading Data from FIFO

First transaction: Get the FIFO_WR_PTR:

```
START;
Send device address + write mode
Send address of FIFO_WR_PTR;
REPEATED_START;
Send device address + read mode
Read FIFO_WR_PTR;
STOP;
```

The central processor evaluates the number of samples to be read from the FIFO:

```
NUM_AVAILABLE_SAMPLES = FIFO_WR_PTR – FIFO_RD_PTR
(Note: pointer wrap around should be taken into account)
NUM_SAMPLES_TO_READ = < less than or equal to NUM_AVAILABLE_SAMPLES >
```

Second transaction: Read `NUM_SAMPLES_TO_READ` **samples from the FIFO**:

```
START;
Send device address + write mode
Send address of FIFO_DATA;
REPEATED_START;
Send device address + read mode
for (i = 0; i < NUM_SAMPLES_TO_READ; i++) {
Read FIFO_DATA;
Save IR[15:8];
Read FIFO_DATA;
Save IR[7:0];
Read FIFO_DATA;
Save R[15:8];
Read FIFO_DATA;
Save R[7:0];
     }
STOP;
```

Third transaction: Write to FIFO_RD_PTR register. If the second transaction was successful, FIFO_RD_PTR points to the next sample in the FIFO, and this third transaction is not necessary. Otherwise, the processor updates the FIFO_RD_PTR appropriately, so that the samples are reread.

```
START;
Send device address + write mode
Send address of FIFO_RD_PTR;
Write FIFO_RD_PTR;
STOP;
```

Mode Configuration (0x06)

REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	REG ADDR	POR STATE	R/W
Mode Configuration	SHDN	RESET			TEMP_EN	MODE[2:0]			0x06	0x00	R/W

Bit 7: Shutdown Control (SHDN)

The part can be put into a power-save mode by setting this bit to one. While in power-save mode, all registers retain their values, and write/read operations function as normal. All interrupts are cleared to zero in this mode.

Bit 6: Reset Control (RESET)

When the RESET bit is set to one, all configuration, threshold, and data registers are reset to their power-on-state. The only exception is writing both RESET and TEMP_EN bits to one at the same time since temperature data registers 0x16 and 0x17 are not cleared. The RESET bit is cleared automatically back to zero after the reset sequence is completed.

Bit 3: Temperature Enable (TEMP_EN)

This is a self-clearing bit which, when set, initiates a single temperature reading from the temperature sensor. This bit is cleared automatically back to zero at the conclusion of the temperature reading when the bit is set to one in heart rate or SpO_2 mode.

Bits 2:0: Mode Control

These bits set the operating state of the MAX30100. Changing modes does not change any other setting, nor does it erase any previously stored data inside the data registers.

Table 3. Mode Control

MODE[2:0]	MODE
000	Unused
001	Reserved (Do not use)
010	HR only enabled
011	SPO_2 enabled
100–111	Unused

SpO2 Configuration (0x07)

REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	REG ADDR	POR STATE	R/W
SPO_2 Configuration		SPO2_HI_RES_EN	Reserved	SPO2_SR[2:0]			LED_PW[1:0]		0x07	0x00	R/W

Bit 6: SpO_2 High Resolution Enable (SPO2_HI_RES_EN)

Set this bit high. The SpO_2 ADC resolution is 16-bit with 1.6ms LED pulse width.

Bit 5: Reserved. Set low (default).

Bit 4:2: SpO_2 Sample Rate Control

These bits define the effective sampling rate, with one sample consisting of one IR pulse/conversion and one RED pulse/conversion.

The sample rate and pulse width are related, in that the sample rate sets an upper bound on the pulse width time. If the user selects a sample rate that is too high for the selected LED_PW setting, the highest possible sample rate will instead be programmed into the register.

Bits 1:0: LED Pulse Width Control

These bits set the LED pulse width (the IR and RED have the same pulse width), and therefore, indirectly set the integration time of the ADC in each sample. The ADC resolution is directly related to the integration time.

Table 4. SpO_2 Sample Rate Control

SPO2_SR[2:0]	SAMPLES (PER SECOND)
000	50
001	100
010	167
011	200
100	400
101	600
110	800
111	1000

Table 5. LED Pulse Width Control

LED_PW[1:0]	PULSE WIDTH (µs)	ADC RESOLUTION (BITS)
00	200	13
01	400	14
10	800	15
11	1600	16

LED Configuration (0x09)

REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	REG ADDR	POR STATE	R/W
LED Configuration	RED_PA[3:0]				IR_PA[3:0]				0x09	0x00	R/W

Bits 7:4: Red LED Current Control

These bits set the current level of the Red LED as in Table 6.

Bits 3:0: IR LED Current Control

These bits set the current level of the IR LED as in Table 6.

Table 6. LED Current Control

Red_PA[3:0] OR IR_PA[3:0]	TYPICAL LED CURRENT (mA)*
0000	0.0
0001	4.4
0010	7.6
0011	11.0
0100	14.2
0101	17.4
0110	20.8
0111	24.0
1000	27.1
1001	30.6
1010	33.8
1011	37.0
1100	40.2
1101	43.6
1110	46.8
1111	50.0

*Actual measured LED current for each part can vary widely due to the proprietary trim methodology.

Temperature Data (0x16–0x17)

REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	REG ADDR	POR STATE	R/W
Temp_Integer	TINT[7:0]								0x16	0x00	R/W
Temp_Fraction					TFRAC[3:0]				0x17	0x00	R/W

Temperature Integer

The on-board temperature ADC output is split into two registers, one to store the integer temperature and one to store the fraction. Both should be read when reading the temperature data, and the following equation shows how to add the two registers together:

$$T_{MEASURED} = T_{INTEGER} + T_{FRACTION}$$

This register stores the integer temperature data in two's complement format, where each bit corresponds to degree Celsius.

Table 7. Temperature Integer

REGISTER VALUE (hex)	TEMPERATURE (°C)
0x00	0
0x00	+1
...	...
0x7E	+126
0x7F	+127
0x80	-128
0x81	-127
...	...
0xFE	-2
0xFF	-1

Temperature Fraction

This register stores the fractional temperature data in increments of 0.0625°C (1/16th of a degree).

If this fractional temperature is paired with a negative integer, it still adds as a positive fractional value (e.g., -128°C + 0.5°C = -127.5°C).

Applications Information

Sampling Rate and Performance

The MAX30100 ADC is a 16-bit sigma delta converter. The ADC sampling rate can be configured from 50sps to 1ksps. The maximum sample rate for the ADC depends on the selected pulse width, which in turn, determines the ADC resolution. For instance, if the pulse width is set to 200µs, then the ADC resolution is 13 bits and all sample rates from 50sps to 1ksps are selectable. However, if the pulse width is set to 1600µs, then only sample rates of 100sps and 50sps can be set. The allowed sample rates for both SpO_2 and HR mode are summarized in Table 8 and Table 9.

Power Considerations

The LEDs in MAX30100 are pulsed with a low duty cycle for power savings, and the pulsed currents can cause ripples in the LED power supply. To ensure these pulses do not translate into optical noise at the LED outputs, the power supply must be designed to handle peak LED current. Ensure that the resistance and inductance from the power supply (battery, DC/DC converter, or LDO) to the device LED+ pins is much smaller than 1Ω, and that there is at least 1µF of power-supply bypass capacitance to a low impedance ground plane. The decoupling capacitor should be located physically as close as possible to the MAX30100 device.

In the heart-rate only mode, the red LED is inactive, and only the IR LED is used to capture optical data and determine the heart rate. This mode allows power savings due to the red LED being off; in addition, the IR_LED+ power supply can be reduced to save power because the forward voltage of the IR LED is significantly less than that of the red LED.

The average I_{DD} and LED current as function of pulse width and sampling rate is summarized in Table 10 to Table 13.

Table 8. SpO_2 Mode (Allowed Settings)

SAMPLES (per second)	PULSE WIDTH (µs)			
	200	400	800	1600
50	O	O	O	O
100	O	O	O	O
167	O	O	O	
200	O	O	O	
400	O	O		
600	O			
800	O			
1000	O			
Resolution (bits)	13	14	15	16

Table 9. Heart-Rate Mode (Allowed Settings)

SAMPLES (per second)	PULSE WIDTH (µs)			
	200	400	800	1600
50	O	O	O	O
100	O	O	O	O
167	O	O	O	
200	O	O	O	
400	O	O		
600	O	O		
800	O	O		
1000	O	O		
Resolution (bits)	13	14	15	16

Table 10. SpO_2 Mode: Average IDD Current (µA) R_PA = 0x3, IR_PA = 0x3

SAMPLES (per second)	PULSE WIDTH (µs)			
	200	400	800	1600
50	628	650	695	782
100	649	691	776	942
167	678	748	887	
200	692	775	940	
400	779	944		
600	865			
800	952			
1000	1037			

Table 11. SpO_2 Mode: Average LED Current (mA) R_PA = 0x3, IR_PA = 0x3

SAMPLES (per second)	PULSE WIDTH (µs)			
	200	400	800	1600
50	0.667	1.332	2.627	5.172
100	1.26	2.516	4.96	9.766
167	2.076	4.145	8.173	
200	2.491	4.93	9.687	
400	4.898	9.765		
600	7.319			
800	9.756			
1000	12.17			

Table 12. Heart-Rate Mode: Average IDD Current (µA) IR_PA = 0x3

SAMPLES (per second)	PULSE WIDTH (µs)			
	200	400	800	1600
50	608	616	633	667
100	617	634	669	740
167	628	658	716	831
200	635	670	739	876
400	671	740	878	
600	707	810		
800	743	881		
1000	779	951		

Table 13. Heart-Rate Mode: Average LED Current (mA) IR_PA = 0x3

SAMPLES (per second)	PULSE WIDTH (µs)			
	200	400	800	1600
50	0.256	0.511	1.020	2.040
100	0.512	1.022	2.040	4.077
167	0.854	1.705	3.404	6.795
200	1.023	2.041	4.074	8.130
400	2.042	4.074	8.123	
600	3.054	6.089		
800	4.070	8.109		
1000	5.079	10.11		

Hardware Interrupt

The active-low interrupt pin pulls low when an interrupt is triggered. The pin is open-drain and requires a pullup resistor or current source to an external voltage supply (up to +5V from GND). The interrupt pin is not designed to sink large currents, so the pullup resistor value should be large, such as 4.7kΩ.

The internal FIFO stores up to 16 samples, so that the system processor does not need to read the data after every sample. Temperature data may be needed to properly interpret SpO_2 data, but the temperature does not need to be sampled very often—once a second or every few seconds should be sufficient. In heart-rate mode temperature information is not necessary.

Table 14. Red LED Current Settings vs. LED Temperature Rise

RED LED CURRENT SETTING	RED LED DUTY CYCLE (% OF LED PULSE WIDTH TO SAMPLE TIME)	ESTIMATED TEMPERATURE RISE (ADD TO TEMPERATURE SENSOR MEASUREMENT) (°C)
0001 (3.1mA)	8	0.1
1111 (35mA)	8	2
0001 (3.1mA)	16	0.3
1111 (35mA)	16	4
0001 (3.1mA)	32	0.6
1111 (35mA)	32	8

Timing for Measurements and Data Collection

Timing in SpO_2 Mode

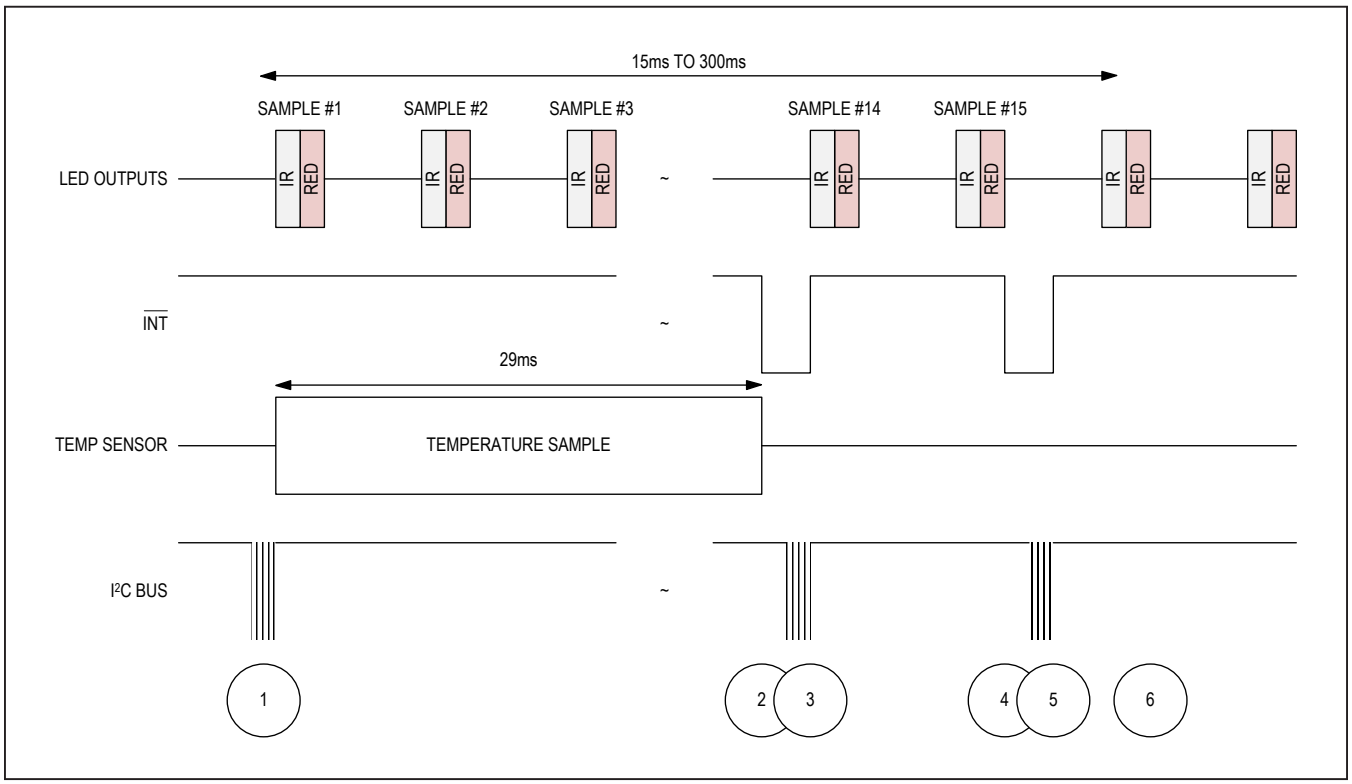


Figure 3. Timing for Data Acquisition and Communication When in SpO_2 Mode

Table 15. Events Sequence for Figure 3 in SpO_2 Mode

EVENT	DESCRIPTION	COMMENTS
1	Enter into SpO_2 mode. Initiate a temperature measurement.	I^2C Write Command Sets MODE[2:0] = 0x03. At the same time, set the TEMP_EN bit to initiate a single temperature measurement. Mask the SPO2_RDY Interrupt.
2	Temperature measurement complete, interrupt generated	TEMP_RDY interrupt triggers, alerting the central processor to read the data.
3	Temp data is read, interrupt cleared	
4	FIFO is almost full, interrupt generated	Interrupt is generated when the FIFO has only one empty space left.
5	FIFO data is read, interrupt cleared	
6	Next sample is stored	New sample is stored at the new read pointer location. Effectively, it is now the first sample in the FIFO.

Timing in Heart-Rate Mode

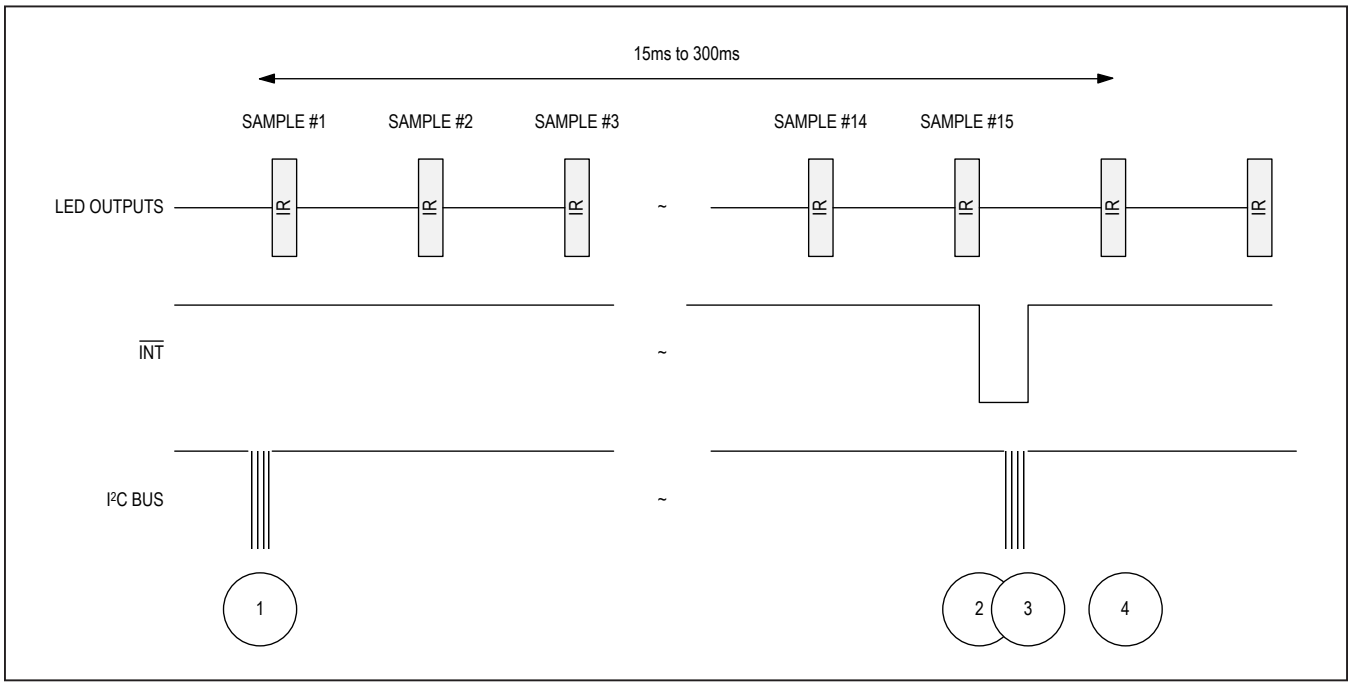


Figure 4. Timing for Data Acquisition and Communication When in Heart Rate Mode

Table 16. Events Sequence for Figure 4 in Heart-Rate Mode

EVENT	DESCRIPTION	COMMENTS
1	Enter into heart rate mode	I2C Write Command Sets MODE[2:0] = 0x02. Mask the HR_RDY interrupt.
2	FIFO is almost full, interrupt generated	Interrupt is generated when the FIFO has only one empty space left.
3	FIFO data is read, interrupt cleared	
4	Next sample is stored	New sample is stored at the new read pointer location. Effectively, it is now the first sample in the FIFO.

Power Sequencing and Requirements

Power-Up Sequencing

Figure 5 shows the recommended power-up sequence for the MAX30100.

It is recommended to power the V_{DD} supply first, before the LED power supplies (R_LED+, IR_LED+). The interrupt and I2C pins can be pulled up to an external voltage even when the power supplies are not powered up.

After the power is established, an interrupt occurs to alert the system that the MAX30100 is ready for operation. Reading the I2C interrupt register clears the interrupt, as shown in Figure 5.

Power-Down Sequencing

The MAX30100 is designed to be tolerant of any power-supply sequencing on power-down.

I2C Interface

The MAX30100 features an I2C/SMBus-compatible, 2-wire serial interface consisting of a serial data line (SDA) and a serial clock line (SCL). SDA and SCL facilitate communication between the MAX30100 and the master at clock rates up to 400kHz. Figure 1 shows the 2-wire interface timing diagram. The master generates SCL and initiates data transfer on the bus. The master device writes data to the MAX30100 by transmitting the proper slave address followed by data. Each transmit sequence is framed by a START (S) or REPEATED START (Sr) condition and a STOP (P) condition. Each word transmitted to the MAX30100 is 8 bits long and is followed by an acknowledge clock pulse. A master reading data from the MAX30100 transmits the proper slave address followed by a series of nine SCL pulses.

The MAX30100 transmits data on SDA in sync with the master-generated SCL pulses. The master acknowledges receipt of each byte of data. Each read sequence is framed by a START (S) or REPEATED START (Sr) condition, a not acknowledge, and a STOP (P) condition. SDA operates as both an input and an open-drain output. A pullup resistor, typically greater than 500Ω, is required on SDA. SCL operates only as an input. A pullup resistor, typically greater than 500Ω, is required on SCL if there are multiple masters on the bus, or if the single master has an open-drain SCL output.

Bit Transfer

One data bit is transferred during each SCL cycle. The data on SDA must remain stable during the high period of the SCL pulse. Changes in SDA while SCL is high are control signals. See the *START and STOP Conditions* section.

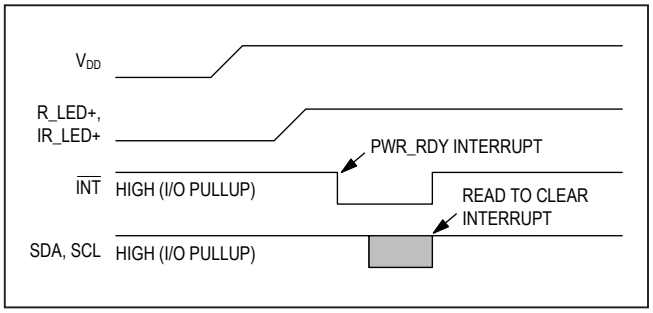


Figure 5. Power-Up Sequence of the Power-Supply Rails

START and STOP Conditions

SDA and SCL idle high when the bus is not in use. A master initiates communication by issuing a START condition. A START condition is a high-to-low transition on SDA with SCL high. A STOP condition is a low-to-high transition on SDA while SCL is high (Figure 6). A START condition from the master signals the beginning of a transmission to the MAX30100. The master terminates transmission, and frees the bus, by issuing a STOP condition. The bus remains active if a REPEATED START condition is generated instead of a STOP condition.

Early STOP Conditions

The MAX30100 recognizes a STOP condition at any point during data transmission except if the STOP condition occurs in the same high pulse as a START condition. For proper operation, do not send a STOP condition during the same SCL high pulse as the START condition.

Slave Address

A bus master initiates communication with a slave device by issuing a START condition followed by the 7-bit slave ID. When idle, the MAX30100 waits for a START condition followed by its slave ID. The serial interface compares each slave ID bit by bit, allowing the interface to power down and disconnect from SCL immediately if an incorrect slave ID is detected. After recognizing a START condition followed by the correct slave ID, the MAX30100 is ready to accept or send data. The LSB of the slave ID word is the Read/$\overline{\text{Write}}$ (R/$\overline{\text{W}}$) bit. R/$\overline{\text{W}}$ indicates whether the master is writing to or reading data from the MAX30100. R/$\overline{\text{W}}$ = 0 selects a write condition, R/$\overline{\text{W}}$ = 1 selects a read condition). After receiving the proper slave ID, the MAX30100 issues an ACK by pulling SDA low for one clock cycle.

The MAX30100 slave ID consists of seven fixed bits, B7–B1 (set to 0b1010111). The most significant slave ID bit (B7) is transmitted first, followed by the remaining bits. Table 18 shows the possible slave IDs of the device.

Acknowledge

The acknowledge bit (ACK) is a clocked 9th bit that the MAX30100 uses to handshake receipt each byte of data when in write mode (Figure 7). The MAX30100 pulls down SDA during the entire master-generated 9th clock pulse if the previous byte is successfully received. Monitoring ACK allows for detection of unsuccessful data transfers. An unsuccessful data transfer occurs if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus master will retry communication. The master pulls down SDA during the 9th clock cycle to acknowledge receipt of data when the MAX30100 is in read mode. An acknowledge is sent by the master after each read byte to allow data transfer to continue. A not-acknowledge is sent when the master reads the final byte of data from the MAX30100, followed by a STOP condition.

Table 17. Slave ID Description

B7	B6	B5	B4	B3	B2	B1	B0	WRITE ADDRESS	READ ADDRESS
1	0	1	0	1	1	1	R/$\overline{\text{W}}$	0xAE	0xAF

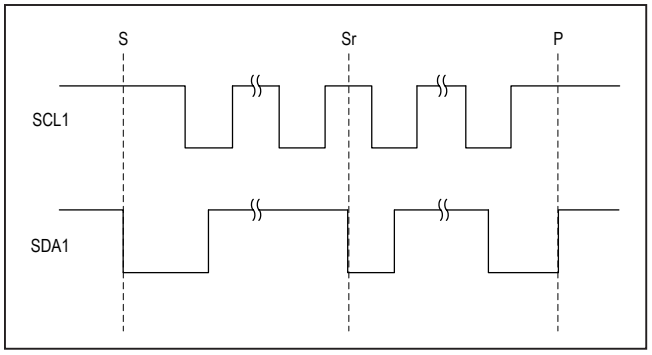


Figure 6. START, STOP, and REPEATED START Conditions

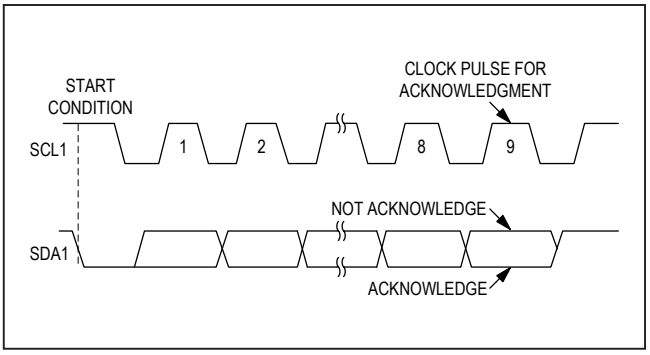


Figure 7. Acknowledge

Write Data Format

For the write operation, send the slave ID as the first byte followed by the register address byte and then one or more data bytes. The register address pointer increments automatically after each byte of data received. For example, the entire register bank can be written by at one time. Terminate the data transfer with a STOP condition. The write operation is shown in Figure 8.

The internal register address pointer increments automatically, so writing additional data bytes fill the data registers in order.

Read Data Format

For the read operation, two I2C operations must be performed. First, the slave ID byte is sent followed by the I2C register that you wish to read. Then a REPEATED START (Sr) condition is sent, followed by the read slave ID. The MAX30100 then begins sending data beginning with the register selected in the first operation. The read pointer increments automatically, so the MAX30100 continues sending data from additional registers in sequential order until a STOP (P) condition is received. The exception to this is the FIFO_DATA register, at which the read pointer no longer increments when reading additional bytes. To read the next register after FIFO_DATA, an I2C write command is necessary to change the location of the read pointer.

An initial write operation is required to send the read register address.

Data is sent from registers in sequential order, starting from the register selected in the initial I2C write operation. If the FIFO_DATA register is read, the read pointer does not automatically increment, and subsequent bytes of data contain the contents of the FIFO.

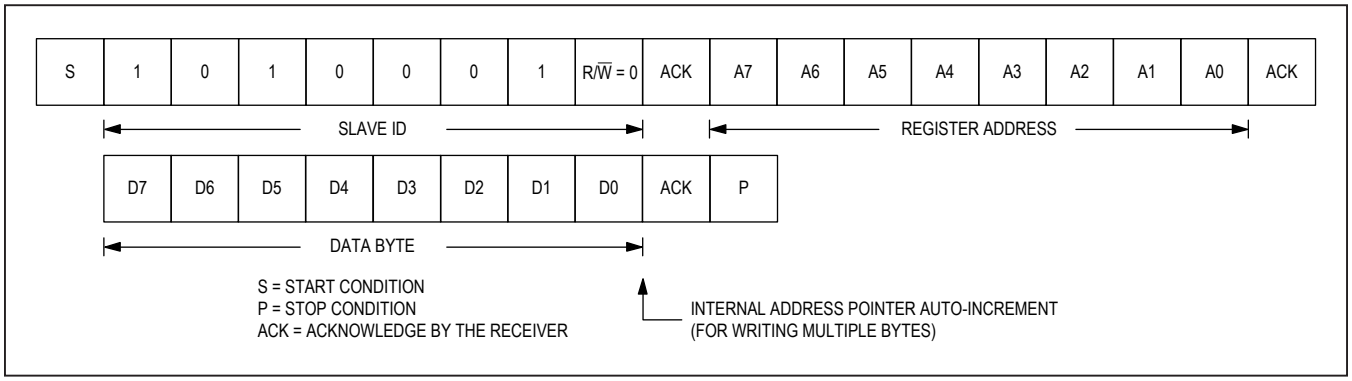


Figure 8. Writing One Data Byte to the MAX30100

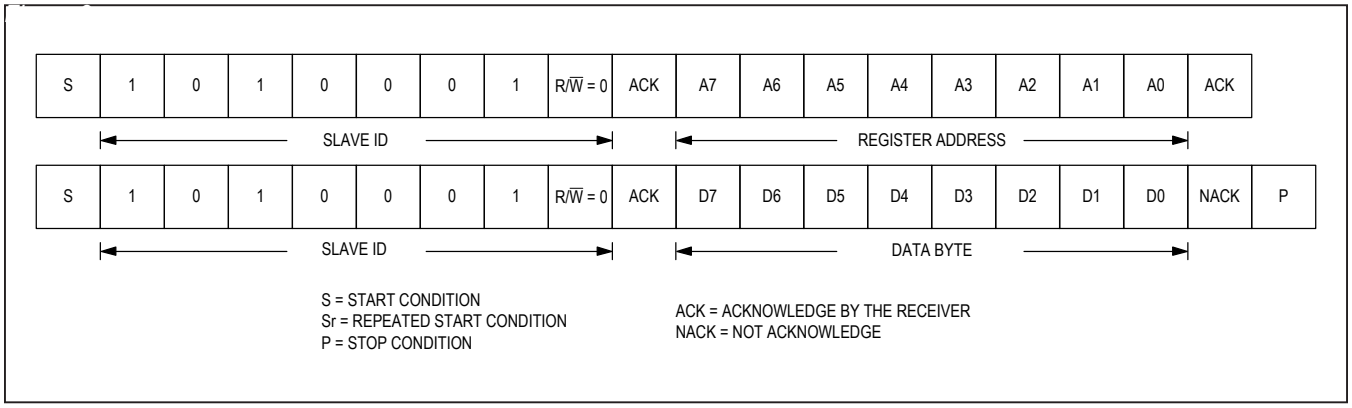


Figure 9. Reading One Byte of Data from the MAX30100

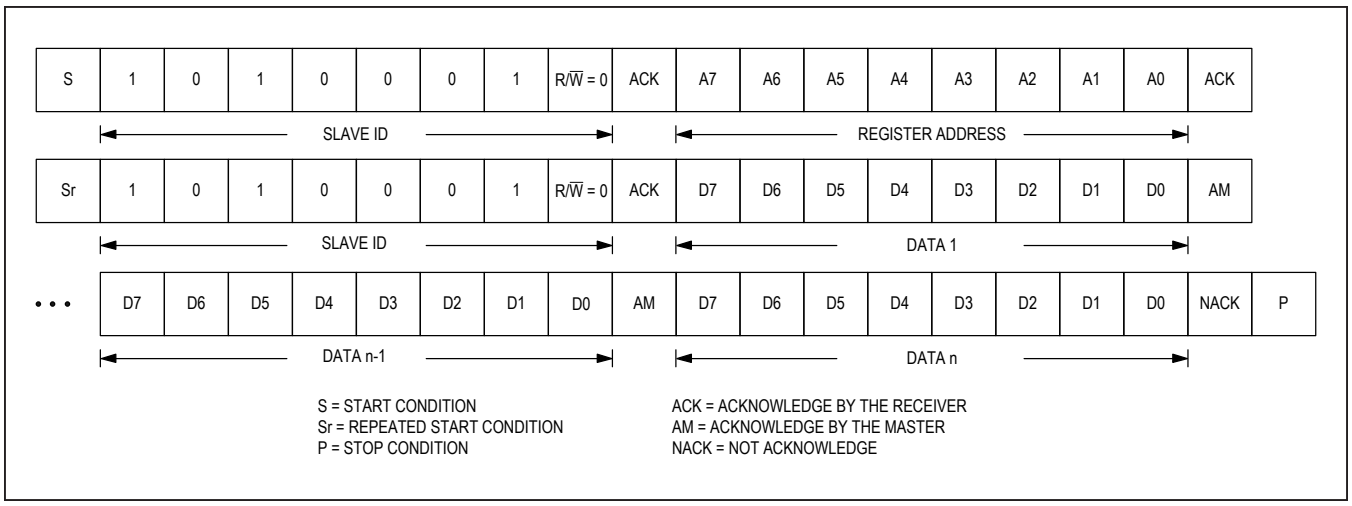
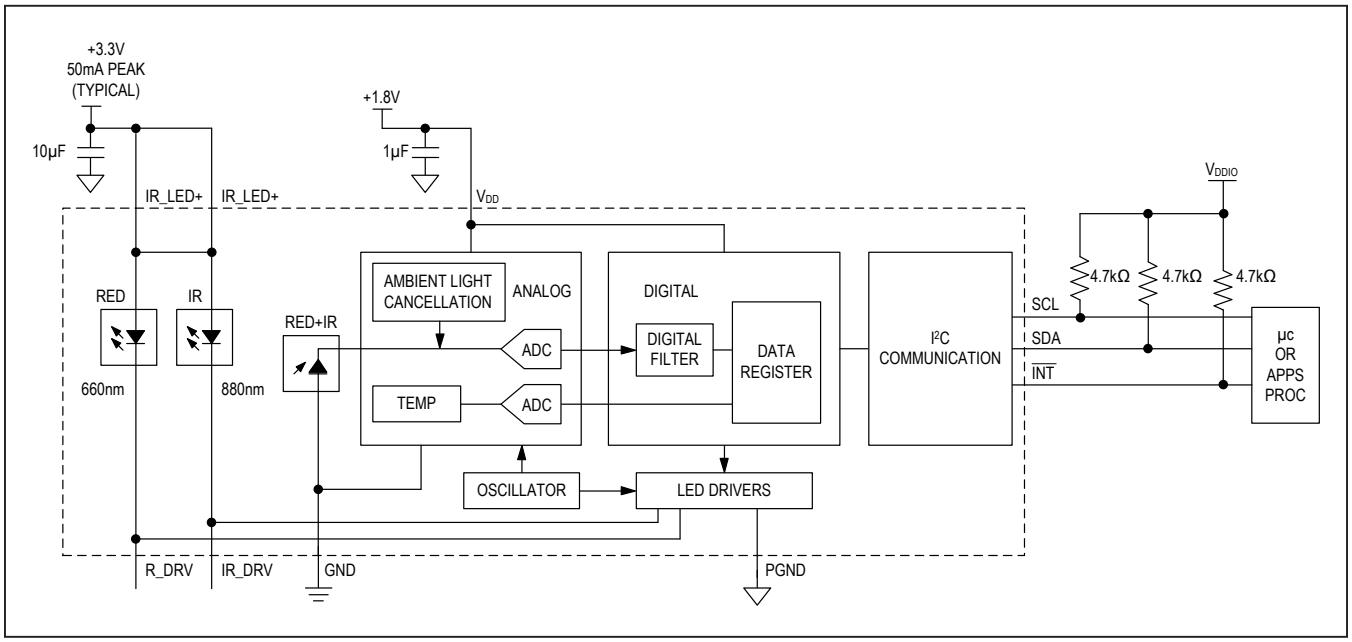


Figure 10. Reading Multiple Bytes of Data from the MAX30100

Typical Application Circuit



Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX30100EFD+	-40°C to +85°C	14 OESIP (0.8mm pitch)

+Denotes a lead(Pb)-free/RoHS-compliant package.

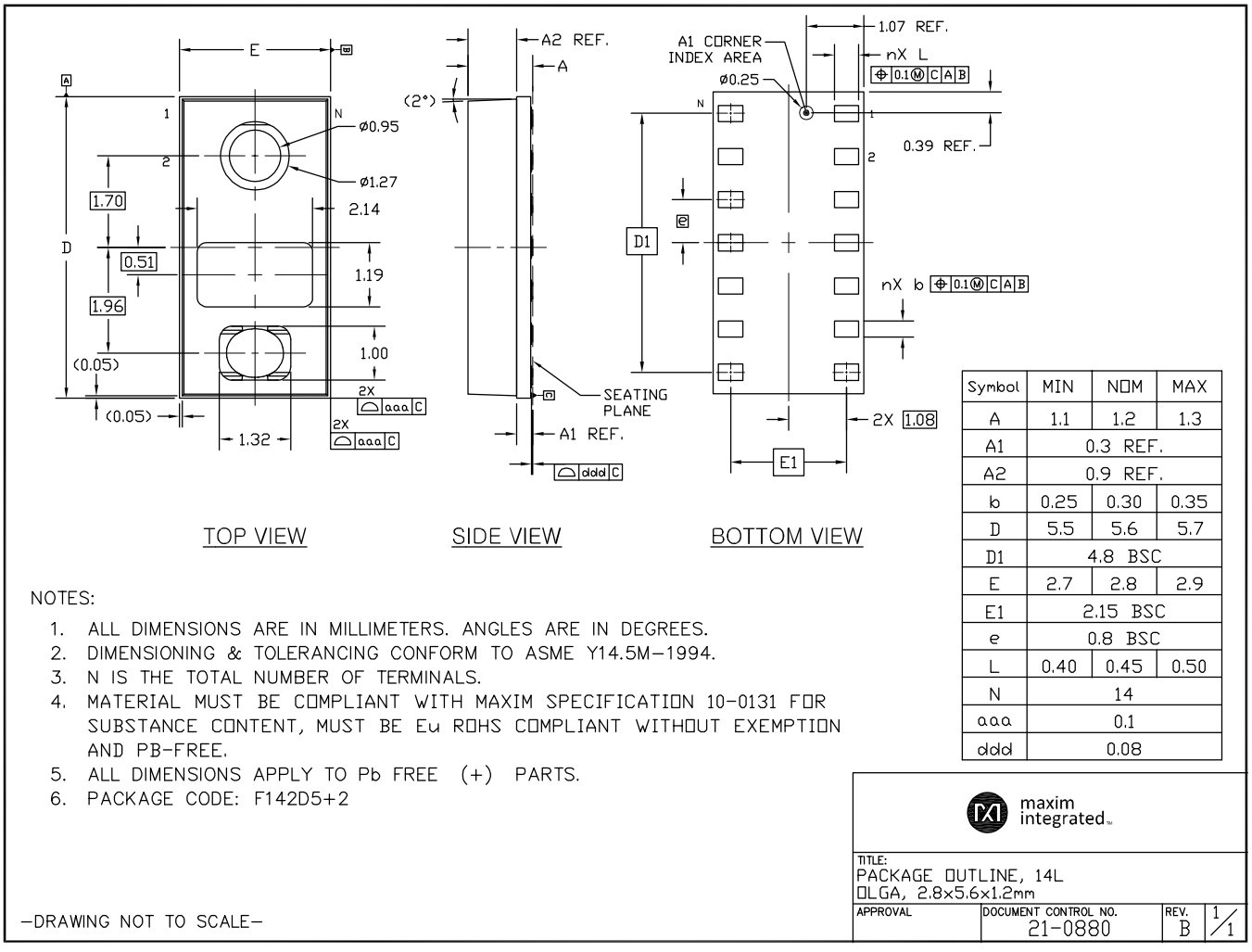
Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
14 OESIP	F142D5+2	21-0880	90-0461



Symbol	MIN	NOM	MAX
A	1.1	1.2	1.3
A1		0.3 REF.	
A2		0.9 REF.	
b	0.25	0.30	0.35
D	5.5	5.6	5.7
D1		4.8 BSC	
E	2.7	2.8	2.9
E1		2.15 BSC	
e		0.8 BSC	
L	0.40	0.45	0.50
N		14	
aaa		0.1	
ddd		0.08	

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
2. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M–1994.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. MATERIAL MUST BE COMPLIANT WITH MAXIM SPECIFICATION 10-0131 FOR SUBSTANCE CONTENT, MUST BE Eu RoHS COMPLIANT WITHOUT EXEMPTION AND PB-FREE.
5. ALL DIMENSIONS APPLY TO Pb FREE (+) PARTS.
6. PACKAGE CODE: F142D5+2

–DRAWING NOT TO SCALE–

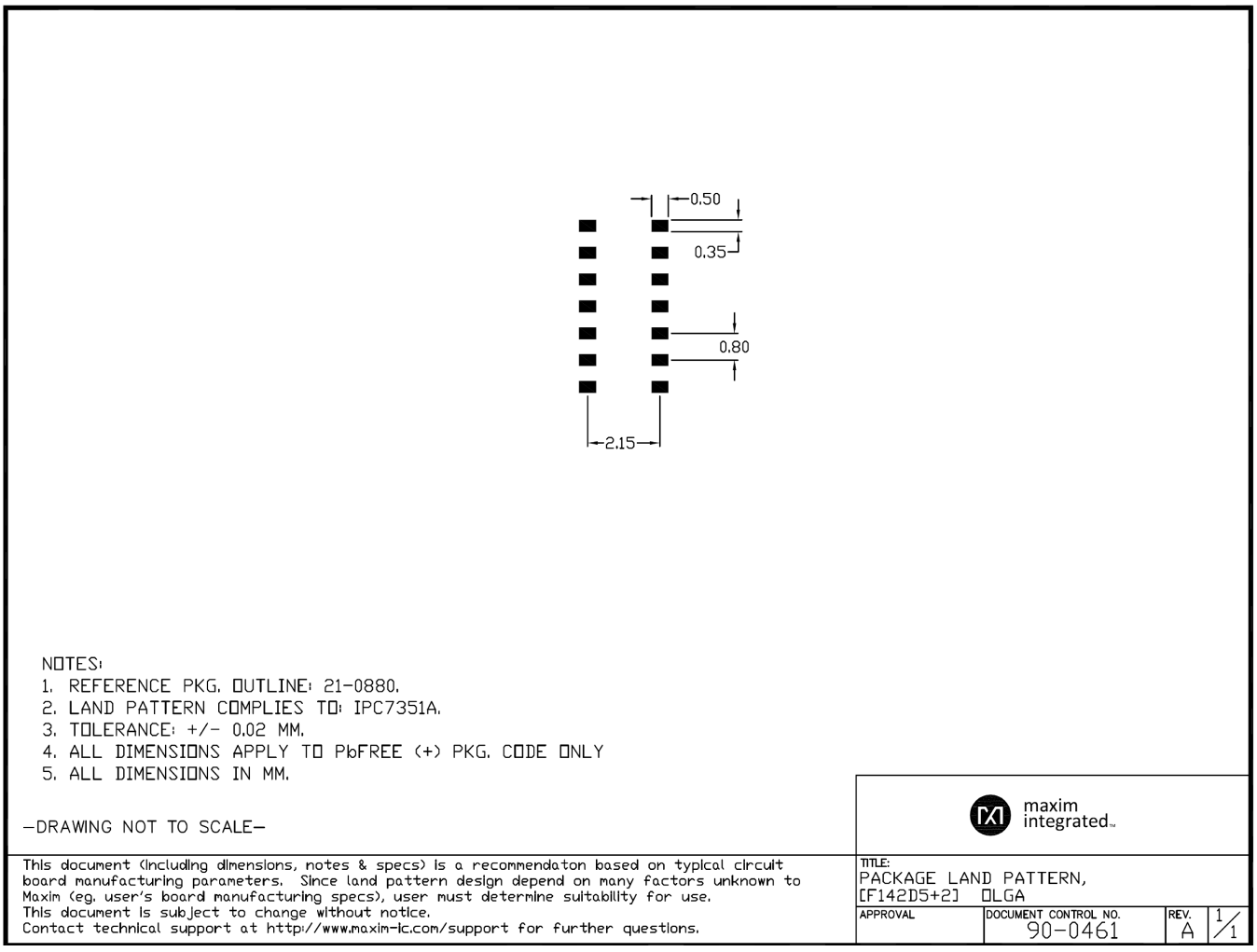
maxim integrated

TITLE:
PACKAGE OUTLINE, 14L
OLGA, 2.8x5.6x1.2mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0880	B	1/1

Package Information (continued)

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.



Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	9/14	Initial release	—

Single-Lead, Heart Rate Monitor Front End

Data Sheet **AD8232**

FEATURES

- Fully integrated single-lead ECG front end
- Low supply current: 170 µA (typical)
- Common-mode rejection ratio: 80 dB (dc to 60 Hz)
- Two or three electrode configurations
- High signal gain (G = 100) with dc blocking capabilities
- 2-pole adjustable high-pass filter
- Accepts up to ±300 mV of half cell potential
- Fast restore feature improves filter settling
- Uncommitted op amp
- 3-pole adjustable low-pass filter with adjustable gain
- Leads off detection: ac or dc options
- Integrated right leg drive (RLD) amplifier
- Single-supply operation: 2.0 V to 3.5 V
- Integrated reference buffer generates virtual ground
- Rail-to-rail output
- Internal RFI filter
- 8 kV HBM ESD rating
- Shutdown pin
- 20-lead 4 mm × 4 mm LFCSP package

APPLICATIONS

- Fitness and activity heart rate monitors
- Portable ECG
- Remote health monitors
- Gaming peripherals
- Biopotential signal acquisition

FUNCTIONAL BLOCK DIAGRAM

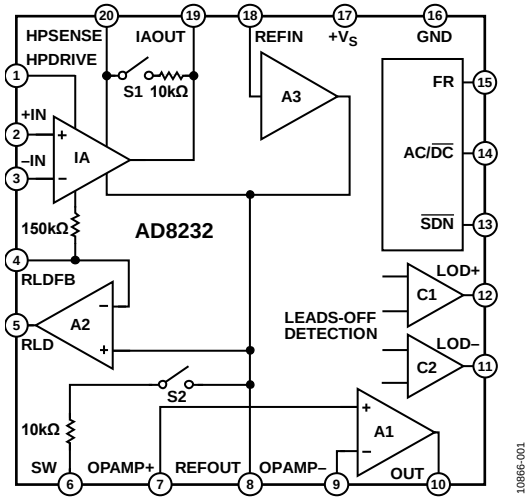


Figure 1.

GENERAL DESCRIPTION

The AD8232 is an integrated signal conditioning block for ECG and other biopotential measurement applications. It is designed to extract, amplify, and filter small biopotential signals in the presence of noisy conditions, such as those created by motion or remote electrode placement. This design allows for an ultralow power analog-to-digital converter (ADC) or an embedded microcontroller to acquire the output signal easily.

The AD8232 can implement a two-pole high-pass filter for eliminating motion artifacts and the electrode half-cell potential. This filter is tightly coupled with the instrumentation architecture of the amplifier to allow both large gain and high-pass filtering in a single stage, thereby saving space and cost.

An uncommitted operational amplifier enables the AD8232 to create a three-pole low-pass filter to remove additional noise. The user can select the frequency cutoff of all filters to suit different types of applications.

To improve common-mode rejection of the line frequencies in the system and other undesired interferences, the AD8232 includes an amplifier for driven lead applications, such as right leg drive (RLD).

The AD8232 includes a fast restore function that reduces the duration of otherwise long settling tails of the high-pass filters. After an abrupt signal change that rails the amplifier (such as a leads off condition), the AD8232 automatically adjusts to a higher filter cutoff. This feature allows the AD8232 to recover quickly, and therefore, to take valid measurements soon after connecting the electrodes to the subject.

The AD8232 is available in a 4 mm × 4 mm, 20-lead LFCSP package. Performance is specified from 0°C to 70°C and is operational from −40°C to +85°C.

Rev. A Document Feedback

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Tel: 781.329.4700
Technical Support www.analog.com

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8/12—Revision 0: Initial Version

SPECIFICATIONS

V_S = 3 V, V_{REF} = 1.5 V, V_{CM} = 1.5 V, T_A = 25°C, FR=low, SDN=high, AC/$\overline{DC}$ = low, unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INSTRUMENTATION AMPLIFIER						
Common-Mode Rejection Ratio, DC to 60 Hz	CMRR	V_{CM} = 0.35 V to 2.85 V, V_{DIFF} = 0 V	80	86		dB
		V_{CM} = 0.35 V to 2.85 V, V_{DIFF} = ±0.3 V		80		dB
Power Supply Rejection Ratio	PSRR	V_S = 2.0 V to 3.5 V	76	90		dB
Offset Voltage (RTI)	V_{OS}					
Instrumentation Amplifier Inputs				3	8	mV
DC Blocking Input[1]				5	50	µV
Average Offset Drift						
Instrumentation Amplifier Inputs				10		µV/°C
DC Blocking Input[1]				0.05		µV/°C
Input Bias Current	I_B			50	200	pA
		T_A = 0°C to 70°C		1		nA
Input Offset Current	I_{OS}			25	100	pA
		T_A = 0°C to 70°C		1		nA
Input Impedance						
Differential				10||7.5		GΩ||pF
Common Mode				5||15		GΩ||pF
Input Voltage Noise (RTI)						
Spectral Noise Density		f = 1 kHz		100		nV/√Hz
Peak-to-Peak Voltage Noise		f = 0.1 Hz to 10 Hz		12		µV p-p
		f = 0.5 Hz to 40 Hz		14		µV p-p
Input Voltage Range		T_A = 0°C to 70°C	0.2		$+V_S$	V
DC Differential Input Range	V_{DIFF}		−300		+300	mV
Output						
Output Swing		R_L = 50 kΩ	0.1		$+V_S$ − 0.1	V
Short-Circuit Current	I_{OUT}			6.3		mA
Gain	A_V			100		V/V
Gain Error		V_{DIFF} = 0 V		0.4		%
		V_{DIFF} = −300 mV to +300 mV		1	3.5	%
Average Gain Drift		T_A = 0°C to 70°C		12		ppm/°C
Bandwidth	BW			2		kHz
RFI Filter Cutoff (Each Input)				1		MHz
OPERATIONAL AMPLIFIER (A1)						
Offset Voltage	V_{OS}			1	5	mV
Average TC		T_A = 0°C to 70°C		5		µV/°C
Input Bias Current	I_B			100		pA
		T_A = 0°C to 70°C		1		nA
Input Offset Current	I_{OS}			100		pA
		T_A = 0°C to 70°C		1		nA
Input Voltage Range			0.1		$+V_S$ − 0.1	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0.5 V to 2.5 V		100		dB
Power Supply Rejection Ratio	PSRR			100		dB
Large Signal Voltage Gain	A_{VO}			110		dB
Output Voltage Range		R_L = 50 kΩ	0.1		$+V_S$ − 0.1	V
Short-Circuit Current Limit	I_{OUT}			12		mA
Gain Bandwidth Product	GBP			100		kHz
Slew Rate	SR			0.02		V/µs
Voltage Noise Density (RTI)	e_n	f = 1 kHz		60		nV/√Hz
Peak-to-Peak Voltage Noise (RTI)	$e_{n\ p\text{-}p}$	f = 0.1 Hz to 10 Hz		6		µV p-p
		f = 0.5 Hz to 40 Hz		8		µV p-p

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
RIGHT LEG DRIVE AMPLIFIER (A2)						
Output Swing		R_L = 50 kΩ	0.1		$+V_S$ − 0.1	V
Short-Circuit Current	I_{OUT}			11		mA
Integrator Input Resistor			120	150	180	kΩ
Gain Bandwidth Product	GDP			100		kHz
REFERENCE BUFFER (A3)						
Offset Error	V_{OS}	R_L > 50 kΩ		1		mV
Input Bias Current	I_B			100		pA
Short-Circuit Current Limit	I_{OUT}			12		mA
Voltage Range		R_L = 50 kΩ	0.1		$+V_S$ − 0.7	V
DC LEADS OFF COMPARATORS						
Threshold Voltage				$+V_S$ − 0.5		V
Hysteresis				60		mV
Propagation Delay				0.5		µs
AC LEADS OFF DETECTOR						
Square Wave Frequency	F_{AC}		50	100	175	kHz
Square Wave Amplitude	I_{AC}			200		nA p-p
Impedance Threshold		Between +IN and −IN	10	20		MΩ
Detection Delay				110		µs
FAST RESTORE CIRCUIT						
Switches		S1 and S2				
On Resistance	R_{ON}		8	10	12	kΩ
Off Leakage				100		pA
Window Comparator						
Threshold Voltage		From either rail		50		mV
Propagation Delay				2		µs
Switch Timing Characteristics						
Feedback Recovery Switch On Time	t_{SW1}			110		ms
Filter Recovery Switch On Time	t_{SW2}			55		ms
Fast Restore Reset	t_{RST}			2		µs
LOGIC INTERFACE						
Input Characteristics						
Input Voltage (AC/$\overline{DC}$ and FR)						
Low	V_{IL}			1.24		V
High	V_{IH}			1.35		V
Input Voltage ($\overline{SDN}$)						
Low	V_{IL}			2.1		V
High	V_{IH}			0.5		V
Output Characteristics		LOD+ and LOD− terminals				
Output Voltage						
Low	V_{OL}			0.05		V
High	V_{OH}			2.95		V
SYSTEM SPECIFICATIONS						
Quiescent Supply Current				170	230	µA
		T_A = 0°C to 70°C		210		µA
Shutdown Current				40	500	nA
		T_A = 0°C to 70°C		100		nA
Supply Range			2.0		3.5	V
Specified Temperature Range			0		70	°C
Operational Temperature Range			−40		+85	°C

[1] Offset referred to the input of the instrumentation amplifier inputs. See the Input Referred Offsets section for additional information.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage	3.6 V
Output Short-Circuit Current Duration	Indefinite
Maximum Voltage, Any Terminal[1]	$+V_S$ + 0.3 V
Minimum Voltage, Any Terminal[1]	−0.3 V
Storage Temperature Range	−65°C to +125°C
Operating Temperature Range	−40°C to +85°C
Maximum Junction Temperature	140°C
θ_{JA} Thermal Impedance[2]	48°C/W
θ_{JC} Thermal Impedance	4.4°C/W
ESD Rating	
Human Body Model (HBM)	8 kV
Charged Device Model (FICDM)	1.25 kV
Machine Model (MM)	200 V

[1] This level or the maximum specified supply voltage, whichever is the lesser, indicates the superior voltage limit for any terminal. If input voltages beyond the specified minimum or maximum voltages are expected, place resistors in series with the inputs to limit the current to less than 5 mA.

[2] θ_{JA} is specified for a device in free air on a 4-layer JEDEC board.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

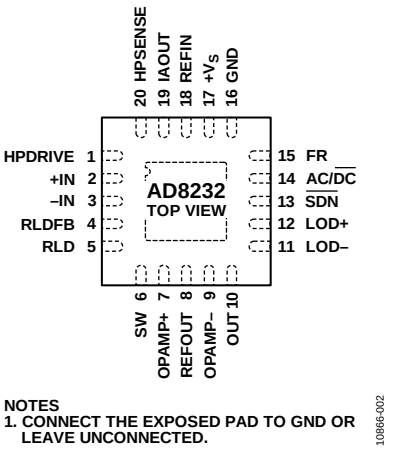

Figure 2. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	HPDRIVE	High-Pass Driver Output. Connect HPDRIVE to the capacitor in the first high-pass filter. The AD8232 drives this pin to keep HPSENSE at the same level as the reference voltage.
2	+IN	Instrumentation Amplifier Positive Input. +IN is typically connected to the left arm (LA) electrode.
3	−IN	Instrumentation Amplifier Negative Input. −IN is typically connected to the right arm (RA) electrode.
4	RLDFB	Right Leg Drive Feedback Input. RLDFB is the feedback terminal for the right leg drive circuit.
5	RLD	Right Leg Drive Output. Connect the driven electrode (typically, right leg) to the RLD pin.
6	SW	Fast Restore Switch Terminal. Connect this terminal to the output of the second high-pass filter.
7	OPAMP+	Operational Amplifier Noninverting Input.
8	REFOUT	Reference Buffer Output. The instrumentation amplifier output is referenced to this potential. Use REFOUT as a virtual ground for any point in the circuit that needs a signal reference.
9	OPAMP−	Operational Amplifier Inverting Input.
10	OUT	Operational Amplifier Output. The fully conditioned heart rate signal is present at this output. OUT can be connected to the input of an ADC.
11	LOD−	Leads Off Comparator Output. In dc leads off detection mode, LOD− is high when the electrode to −IN is disconnected, and it is low when connected. In ac leads off detection mode, LOD− is always low.
12	LOD+	Leads Off Comparator Output. In dc leads off detection mode, LOD+ is high when the +IN electrode is disconnected, and it is low when connected. In ac leads off detection mode, LOD+ is high when either the −IN or +IN electrode is disconnected, and it is low when both electrodes are connected.
13	$\overline{\text{SDN}}$	Shutdown Control Input. Drive $\overline{\text{SDN}}$ low to enter the low power shutdown mode.
14	AC/$\overline{\text{DC}}$	Leads Off Mode Control Input. Drive the AC/$\overline{\text{DC}}$ pin low for dc leads off mode. Drive the AC/$\overline{\text{DC}}$ pin high for ac leads off mode.
15	FR	Fast Restore Control Input. Drive FR high to enable fast recovery mode; otherwise, drive it low.
16	GND	Power Supply Ground.
17	$+V_S$	Power Supply Terminal.
18	REFIN	Reference Buffer Input. Use REFIN, a high impedance input terminal, to set the level of the reference buffer.
19	IAOUT	Instrumentation Amplifier Output Terminal.
20	HPSENSE	High-Pass Sense Input for Instrumentation Amplifier. Connect HPSENSE to the junction of R and C that sets the corner frequency of the dc blocking circuit.
	EP	Exposed Pad. Connect the exposed pad to GND or leave it unconnected.

TYPICAL PERFORMANCE CHARACTERISTICS

V_S = 3 V, V_{REF} = 1.5 V, V_{CM} = 1.5 V, T_A = 25°C, unless otherwise noted.

INSTRUMENTATION AMPLIFIER PERFORMANCE CURVES

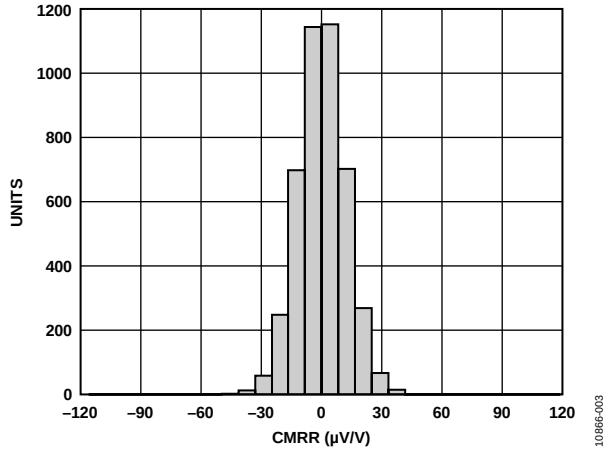

Figure 3. Instrumentation Amplifier CMRR Distribution

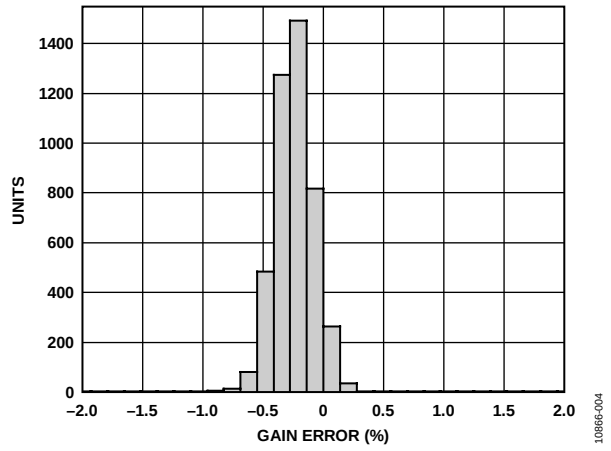

Figure 4. Instrumentation Amplifier Gain Error Distribution

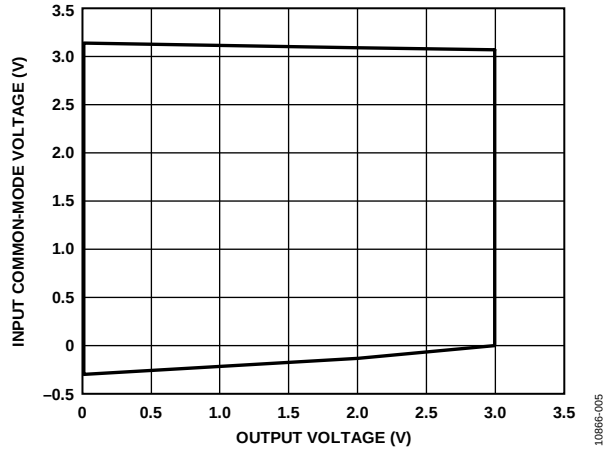

Figure 5. Instrumentation Amplifier
Input Common-Mode Range vs. Output Voltage

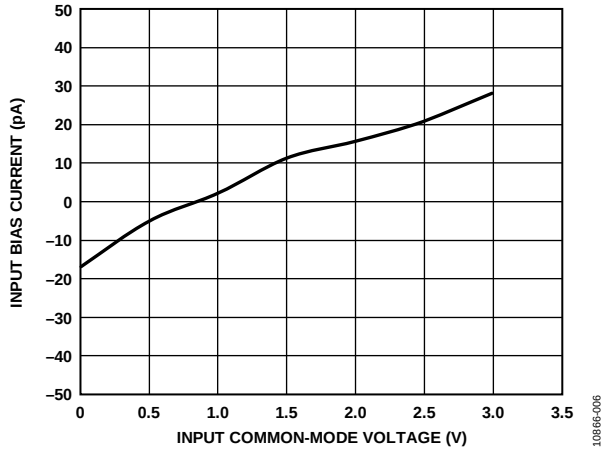

Figure 6. Instrumentation Amplifier Input Bias Current vs. CMV

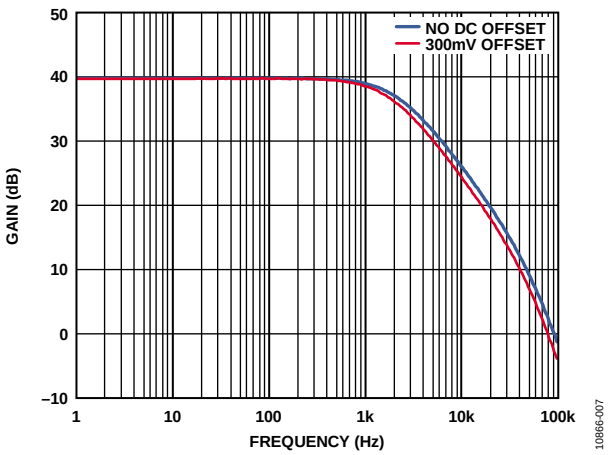

Figure 7. Instrumentation Amplifier Gain vs. Frequency

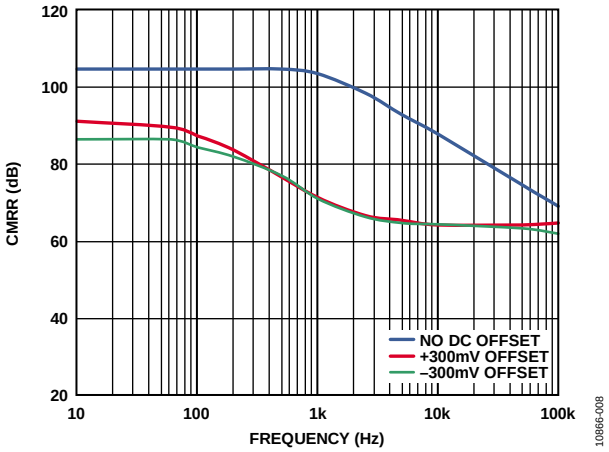

Figure 8. Instrumentation Amplifier CMRR vs. Frequency, RTI

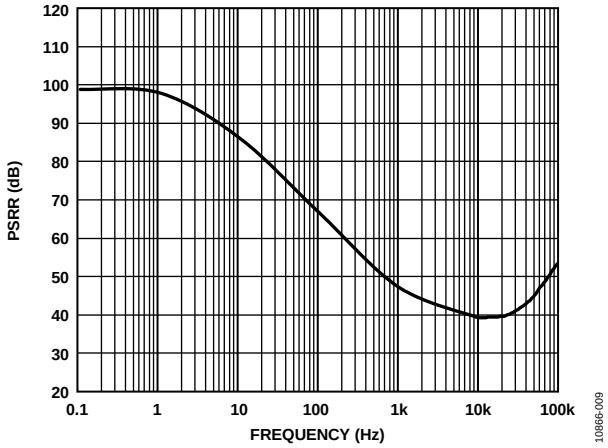

Figure 9. Instrumentation Amplifier PSRR vs. Frequency

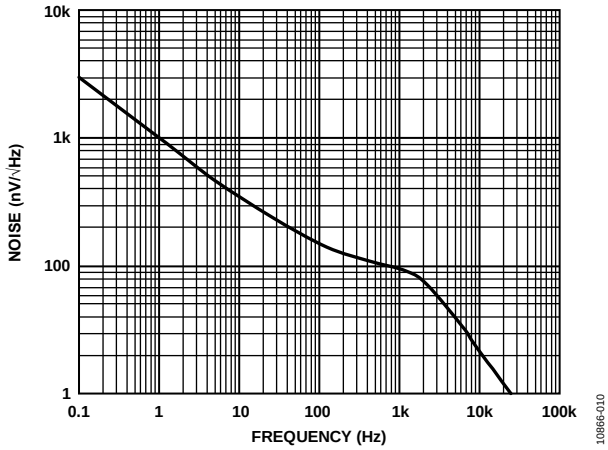

Figure 10. Instrumentation Amplifier Voltage Noise Spectral Density (RTI)

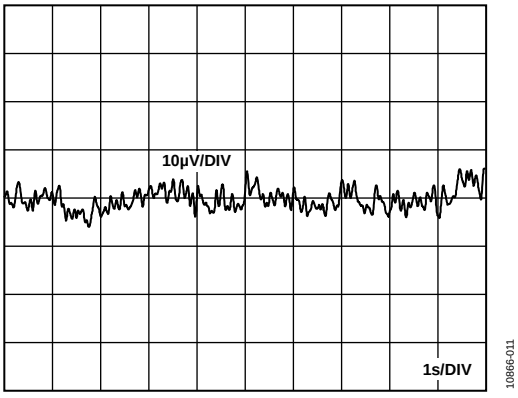

Figure 11. Instrumentation Amplifier 0.1 Hz to 10 Hz Noise

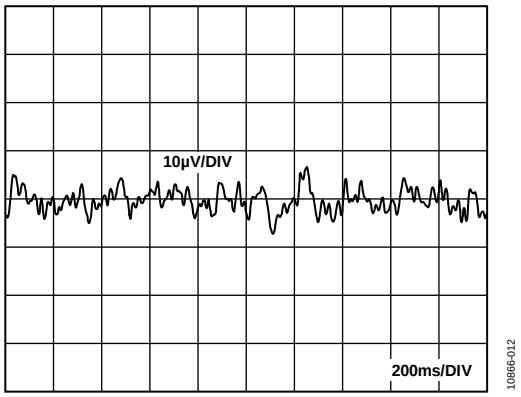

Figure 12. Instrumentation Amplifier 0.5 Hz to 40 Hz Noise

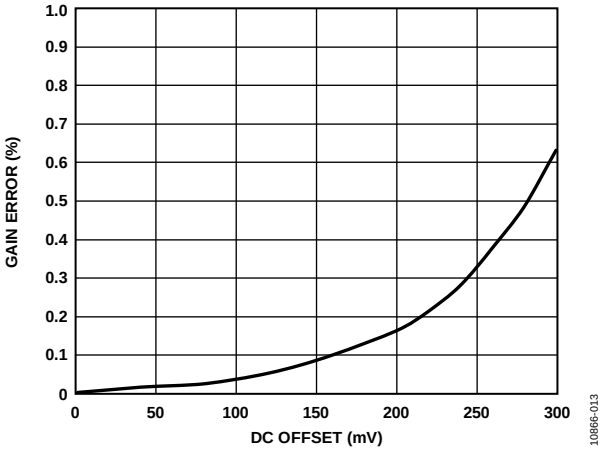

Figure 13. Instrumentation Amplifier Gain Error vs. DC Offset

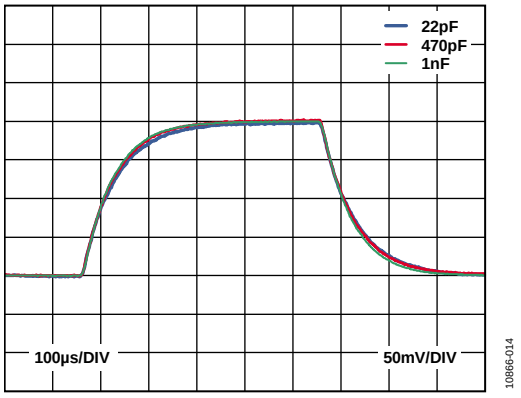

Figure 14. Instrumentation Amplifier Small Signal Pulse Response

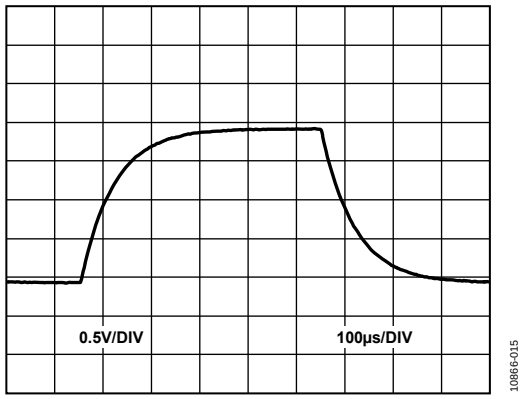

Figure 15. Instrumentation Amplifier Large Signal Pulse Response

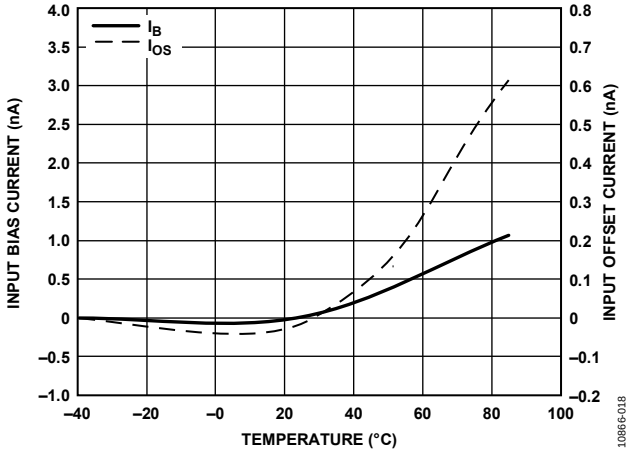

Figure 18. Instrumentation Amplifier Input Bias Current and Input Offset Current vs. Temperature

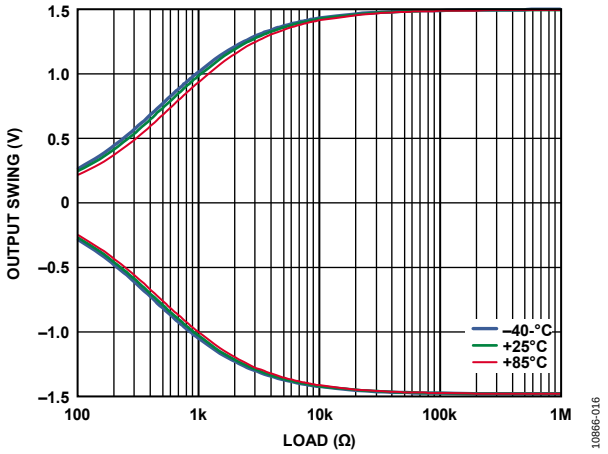

Figure 16. Instrumentation Amplifier Output Swing vs. Load

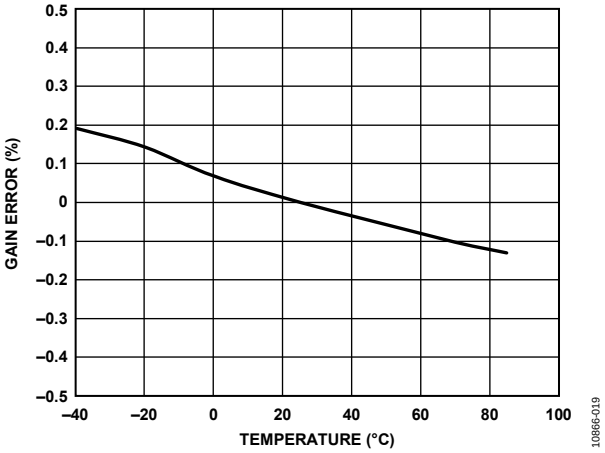

Figure 19. Instrumentation Amplifier Gain Error vs. Temperature

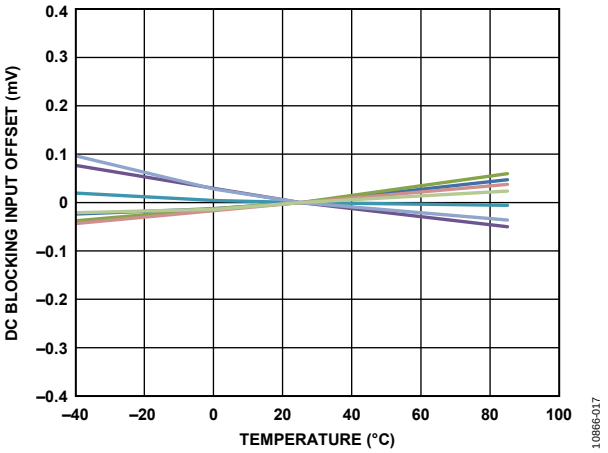

Figure 17. Instrumentation Amplifier DC Blocking Input Offset Drift

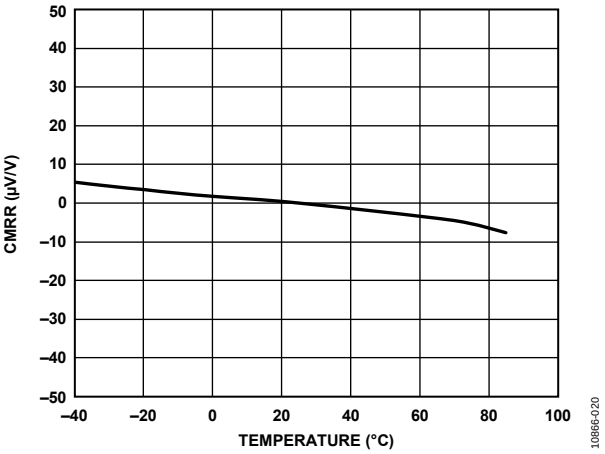

Figure 20. Instrumentation Amplifier CMRR vs. Temperature

OPERATIONAL AMPLIFIER PERFORMANCE CURVES

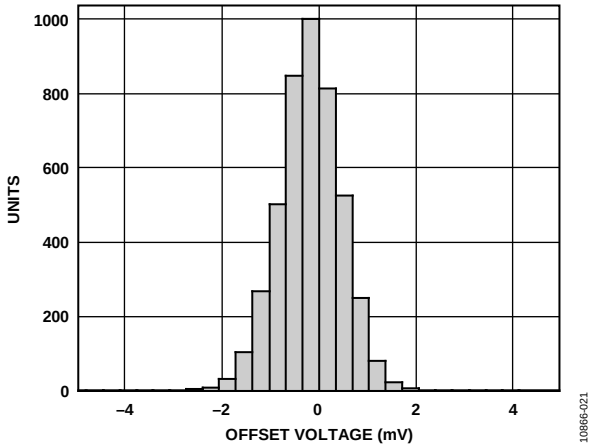

Figure 21. Operational Amplifier Offset Distribution

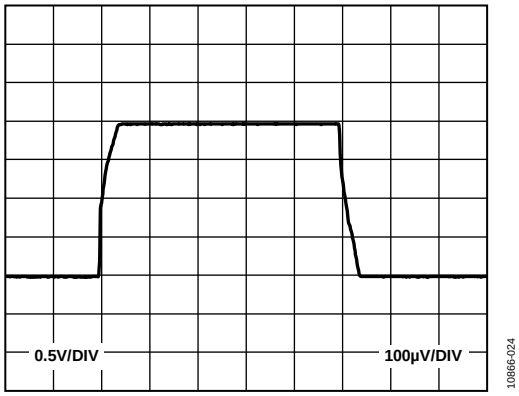

Figure 24. Operational Amplifier Large Signal Transient Response

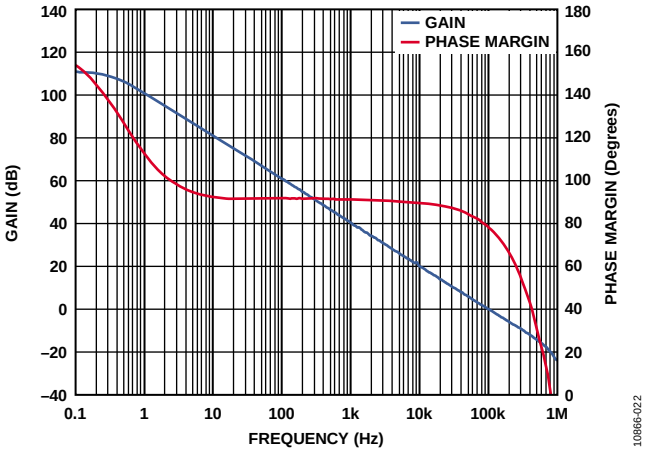

Figure 22. Operational Amplifier Open-Loop Gain and Phase vs. Frequency

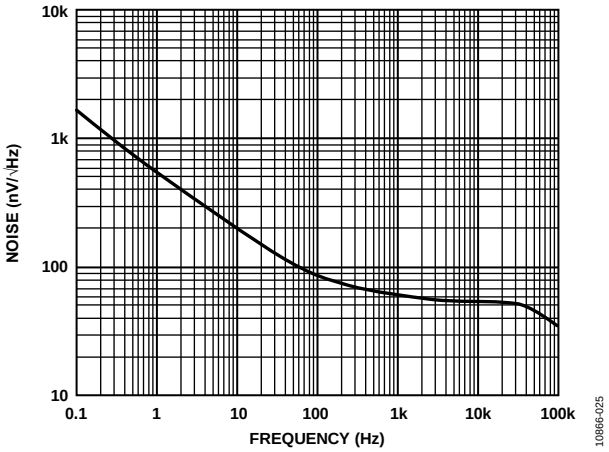

Figure 25. Operational Amplifier Voltage Spectral Noise Density vs. Frequency

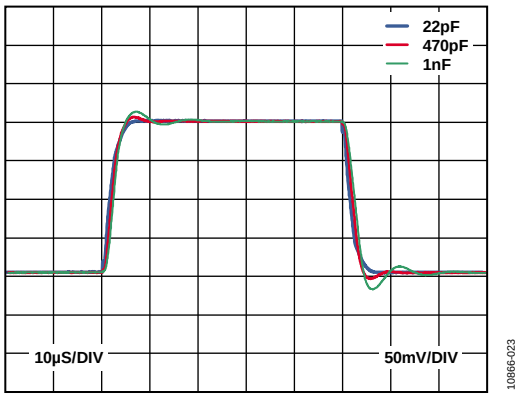

Figure 23. Operational Amplifier Small Signal Response for Various Capacitive Loads

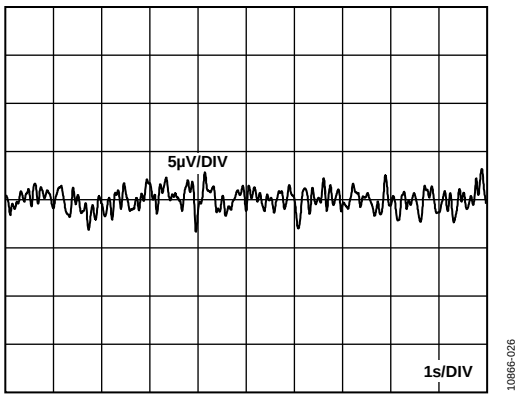

Figure 26. Operational Amplifier 0.1 Hz to 10 Hz Noise

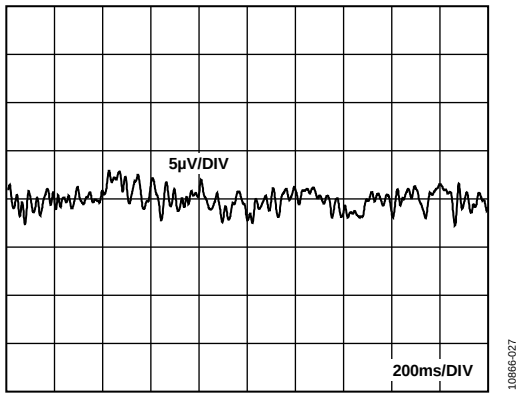

Figure 27. Operational Amplifier 0.5 Hz to 40 Hz Noise

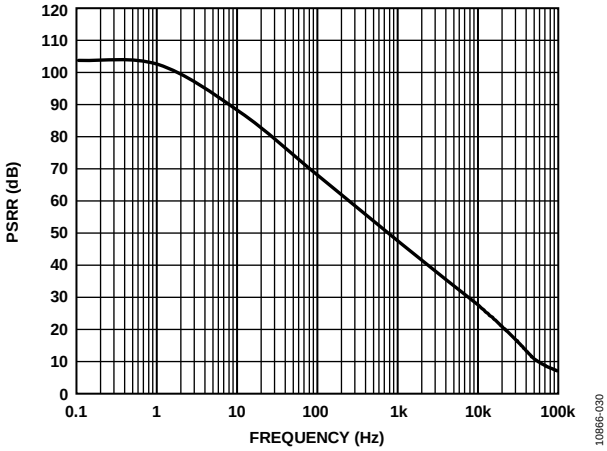

Figure 30. Operational Amplifier Power Supply Rejection Ratio

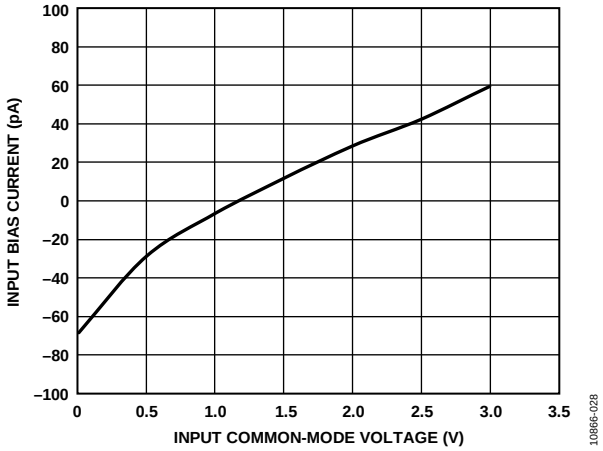

Figure 28. Operational Amplifier Bias Current vs. Input Common-Mode Voltage

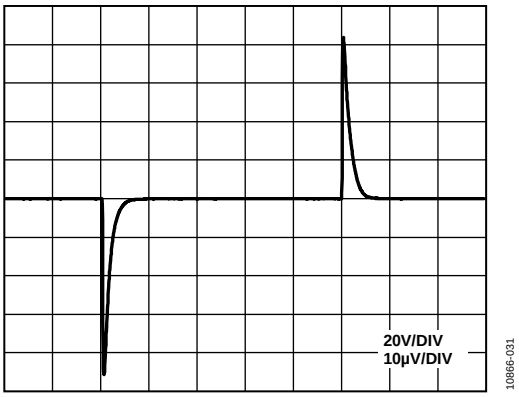

Figure 31. Operational Amplifier Load Transient Response (100 µA Load Change)

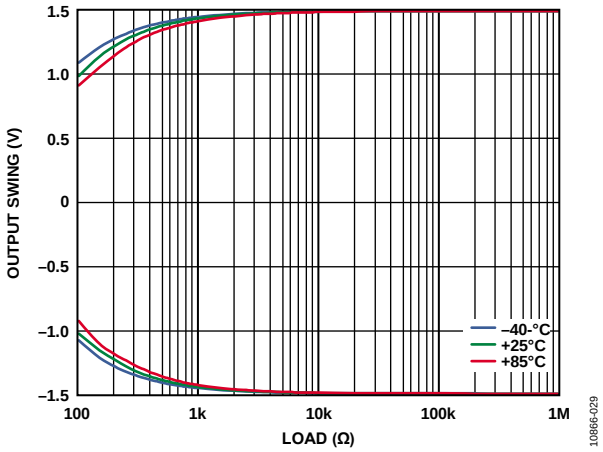

Figure 29. Operational Amplifier Output Voltage Swing vs. Output Current

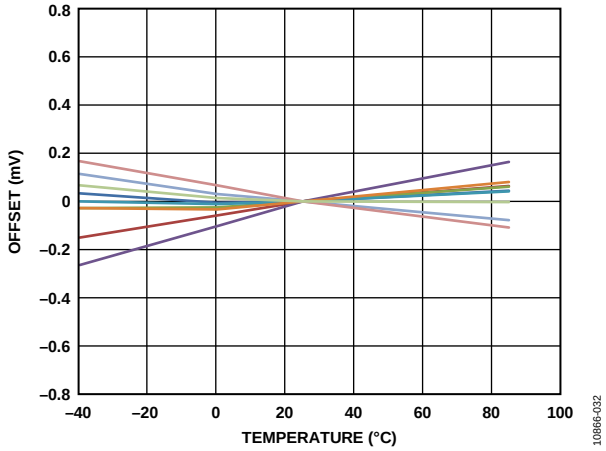

Figure 32. Operational Amplifier Offset vs. Temperature

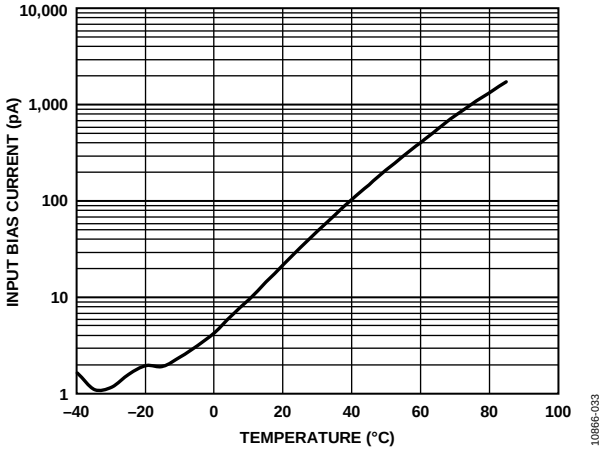

Figure 33. Operational Amplifier Bias Current vs. Temperature

RIGHT LEG DRIVE (RLD) AMPLIFIER PERFORMANCE CURVES

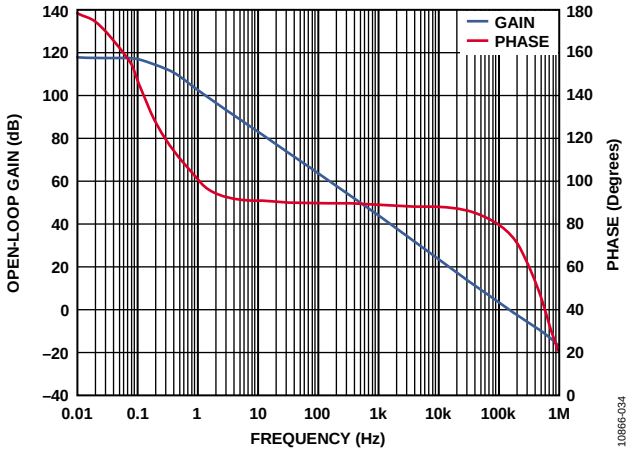

Figure 34. RLD Amplifier Open-Loop Gain and Phase vs. Frequency

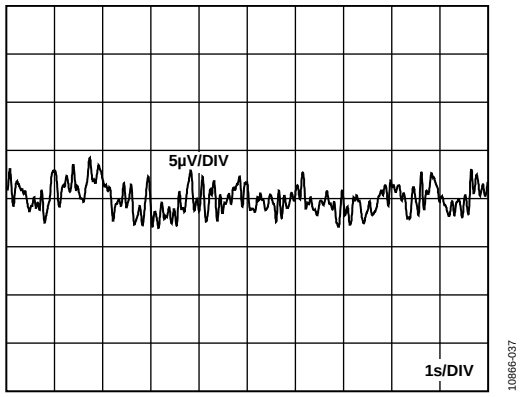

Figure 37. RLD Amplifier 0.1 Hz to 10 Hz Noise

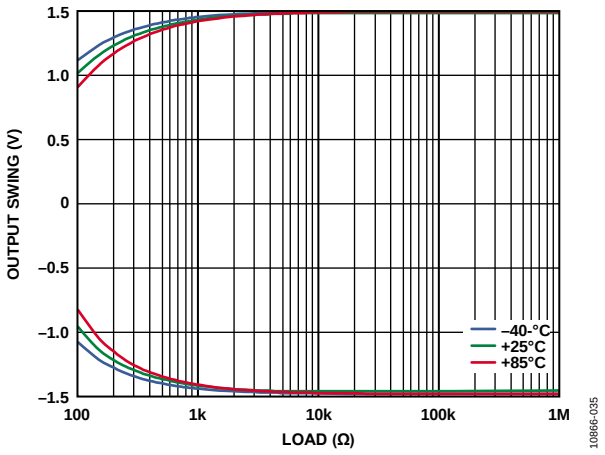

Figure 35. RLD Amplifier Output Voltage Swing vs. Output Current

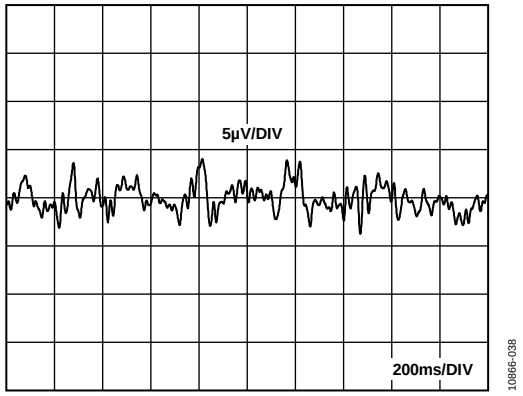

Figure 38. RLD Amplifier 0.5 Hz to 40 Hz Noise

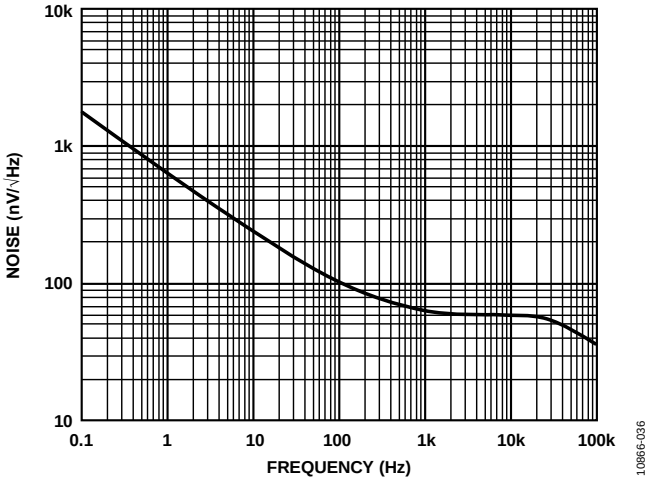

Figure 36. RLD Amplifier Voltage Spectral Noise Density vs. Frequency

REFERENCE BUFFER PERFORMANCE CURVES

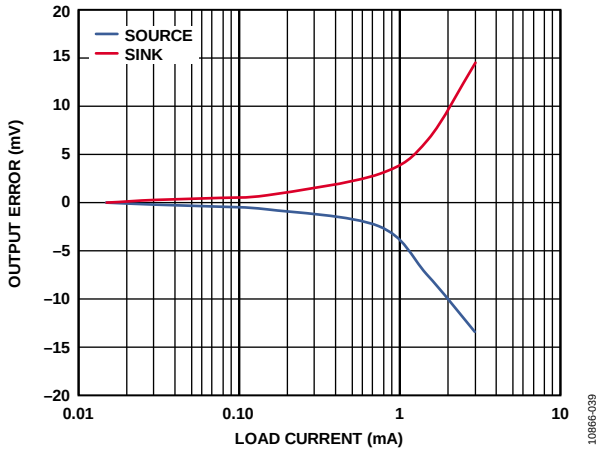

Figure 39. Reference Buffer Load Regulation

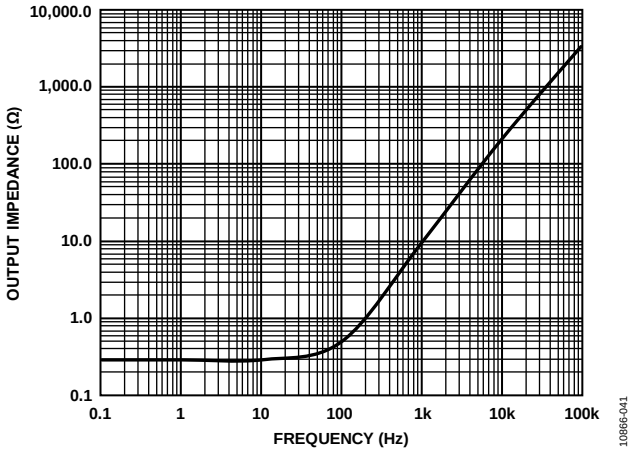

Figure 41. Reference Buffer Output Impedance vs. Frequency

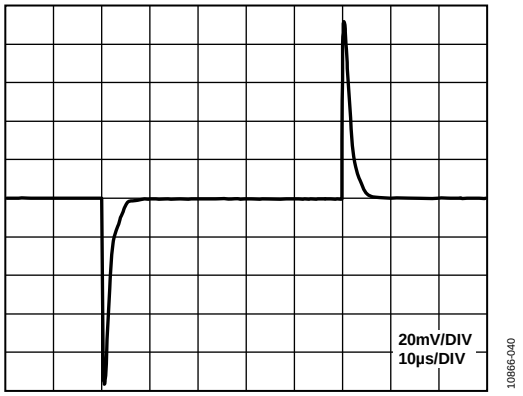

Figure 40. Reference Buffer Load Transient Response (100 µA Load Change)

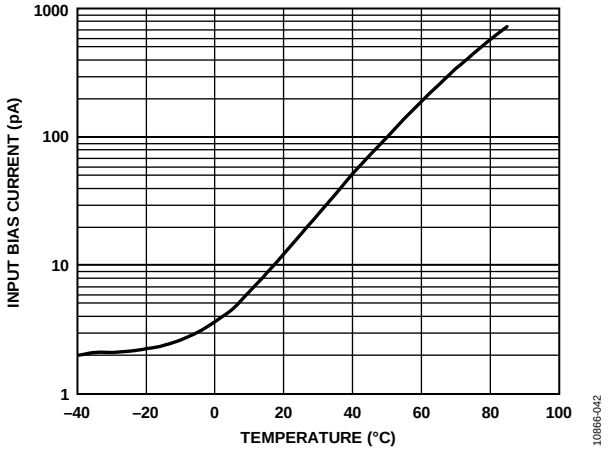

Figure 42. Reference Buffer Bias Current vs. Temperature

SYSTEM PERFORMANCE CURVES

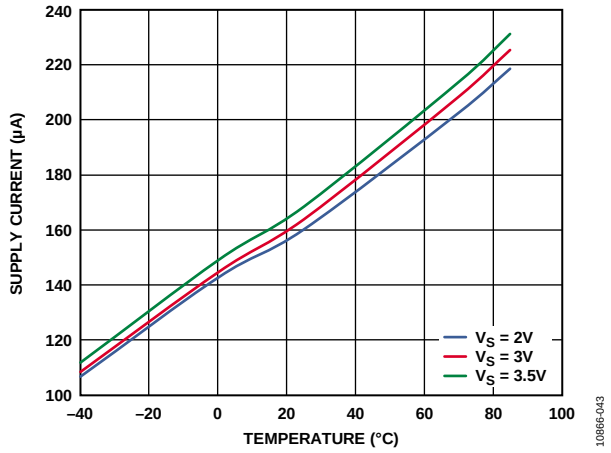

Figure 43. Supply Current vs. Temperature

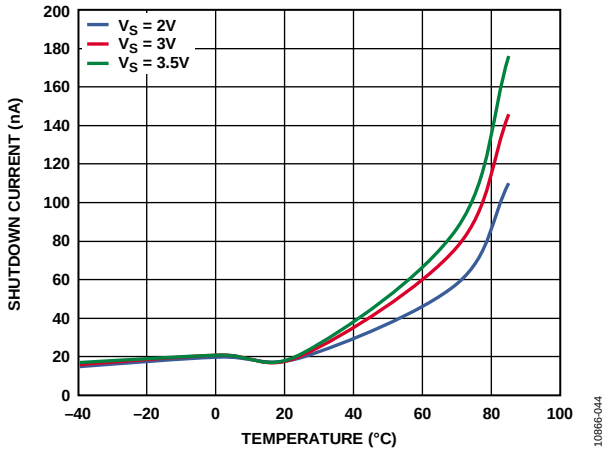

Figure 44. Shutdown Current vs. Temperature

THEORY OF OPERATION

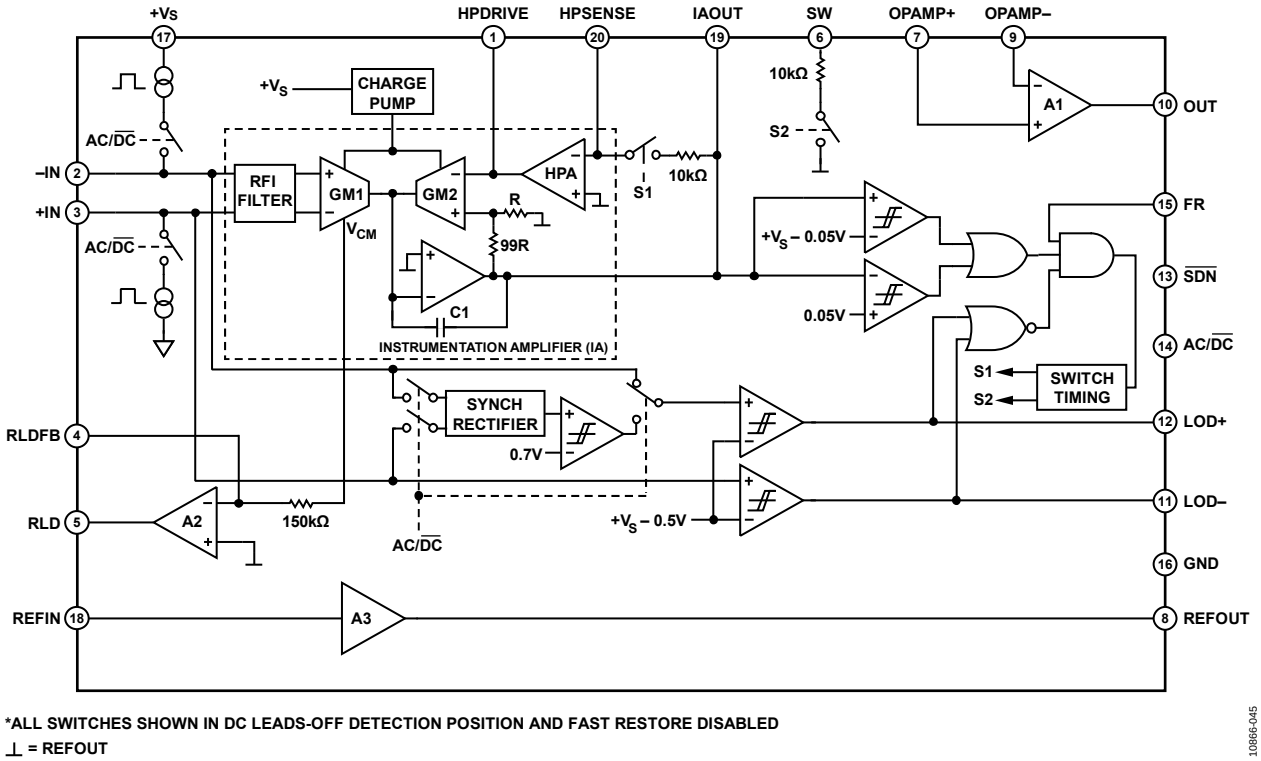

Figure 45. Simplified Schematic Diagram

ARCHITECTURE OVERVIEW

The AD8232 is an integrated front end for signal conditioning of cardiac biopotentials for heart rate monitoring. It consists of a specialized instrumentation amplifier (IA), an operational amplifier (A1), a right leg drive amplifier (A2), and a midsupply reference buffer (A3). In addition, the AD8232 includes leads off detection circuitry and an automatic fast restore circuit that brings back the signal shortly after leads are reconnected.

The AD8232 contains a specialized instrumentation amplifier that amplifies the ECG signal while rejecting the electrode half-cell potential on the same stage. This is possible with an indirect current feedback architecture, which reduces size and power compared with traditional implementations

INSTRUMENTATION AMPLIFIER

The instrumentation amplifier is shown in Figure 45 as comprised by two well-matched transconductance amplifiers (GM1 and GM2), the dc blocking amplifier (HPA), and an integrator formed by C1 and an op amp. The transconductance amplifier, GM1, generates a current that is proportional to the voltage present at its inputs. When the feedback is satisfied, an equal voltage appears across the inputs of the transconductance amplifier, GM2, thereby matching the current generated by GM1. The difference generates an error current that is integrated across Capacitor C1. The resulting voltage appears at the output of the instrumentation amplifier.

The feedback of the amplifier is applied via GM2 through two separate paths: the two resistors divide the output signal to set an overall gain of 100, whereas the dc blocking amplifier integrates any deviation from the reference level. Consequently, dc offsets as large as ±300 mV across the GM1 inputs appear inverted and with the same magnitude across the inputs of GM2, all without saturating the signal of interest.

To increase the common-mode voltage range of the instrumentation amplifier, a charge pump boosts the supply voltage for the two transconductance amplifiers. This further prevents saturation of the amplifier in the presence of large common-mode signals, such as line interference. The charge pump runs from an internal oscillator, the frequency of which is set around 500 kHz.

OPERATIONAL AMPLIFIER

This general-purpose operational amplifier (A1) is a rail-to-rail device that can be used for low-pass filtering and to add additional gain. The following sections provide details and example circuits that use this amplifier.

RIGHT LEG DRIVE AMPLIFIER

The right leg drive (RLD) amplifier inverts the common-mode signal that is present at the instrumentation amplifier inputs. When the right leg drive output current is injected into the subject, it counteracts common-mode voltage variations, thus improving the common-mode rejection of the system.

The common-mode signal that is present across the inputs of the instrumentation amplifier is derived from the transconductance amplifier, GM1. It is then connected to the inverting input of A2 through a 150 kΩ resistor.

An integrator can be built by connecting a capacitor between the RLD FB and RLD terminals. A good starting point is a 1 nF capacitor, which places the crossover frequency at about 1 kHz (the frequency at which the amplifier has an inverting unity gain). This configuration results in about 26 dB of loop gain available at a frequency range from 50 Hz to 60 Hz for common-mode line rejection. Higher capacitor values reduce the crossover frequency, thereby reducing the gain that is available for rejection and, consequently, increasing the line noise. Lower capacitor values move the crossover frequency to higher frequencies, allowing increased gain. The tradeoff is that with higher gain, the system can become unstable and saturate the output of the right leg amplifier.

Note that when using this amplifier to drive an electrode, there should be a resistor in series with the output to limit the current to be always less than 10uA even in fault conditions. For example, if the supply used is 3.0V, this resistor should be greater than 330kΩ to account for component and supply variations.

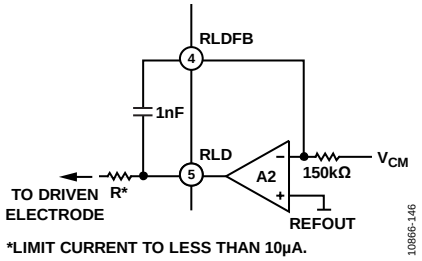

Figure 46. Typical Configuration of Right-Leg Drive Circuit

In two-electrode configurations, RLD can be used to bias the inputs through 10MΩ resistors as described in the Leads Off Detection section. If left unused, it is recommended to configure A2 as a follower by connecting RLDFB directly to RLD.

REFERENCE BUFFER

The AD8232 operates from a single supply. To simplify the design of single-supply applications, the AD8232 includes a reference buffer to create a virtual ground between the supply voltage and the system ground. The signals present at the output of the instrumentation amplifier are referenced around this voltage. For example, if there is zero differential input voltage, the voltage at the output of the instrumentation amplifier is this reference voltage.

The reference voltage level is set at the REFIN pin. It can be set with a voltage divider or by driving the REFIN pin from some other point in the circuit (for example, from the ADC reference). The voltage is available at the REFOUT pin for the filtering circuits or for an ADC input.

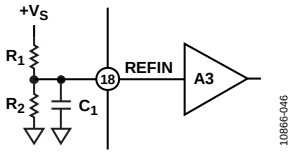

Figure 47. Setting the Internal Reference

To limit the power consumption of the voltage divider, the use of large resistors is recommended, such as 10 MΩ. The designer must keep in mind that high resistor values make it easier for interfering signals to appear at the input of the reference buffer. To minimize noise pickup, it is recommended to place the resistors close to each other and as near as possible to the REFIN terminal. Furthermore, use a capacitor in parallel with the lower resistor on the divider for additional filtering, as shown in Figure 47. Keep in mind that a large capacitor results in better noise filtering but it takes longer to settle the reference after power-up. The total time it takes the reference to settle within 1% can be estimated with the formula

$$t_{SETTLE\_REFERENCE} = 5 \times \frac{R1R2C1}{R1 + R2}$$

Note that disabling the AD8232 with the shutdown terminal does not discharge this capacitor.

FAST RESTORE CIRCUIT

Because of the low cutoff frequency used in high-pass filters in ECG applications, signals may require several seconds to settle. This settling time can result in a frustrating delay for the user after a step response: for example, when the electrodes are first connected.

This fast restore function is implemented internally, as shown in Figure 48. The output of the instrumentation amplifier is connected to a window comparator. The window comparator detects a saturation condition at the output of the instrumentation amplifier when its voltage approaches 50 mV from either supply rail.

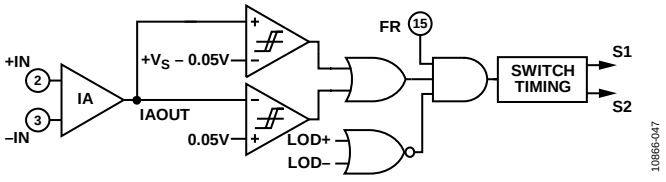

Figure 48. Fast Restore Circuit

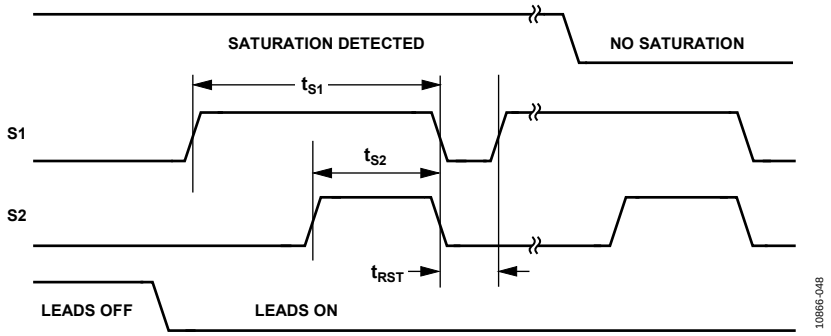

Figure 49. Timing Diagram for Fast Restore Switches (Time Base Not to Scale)

If this saturation condition is present when both input electrodes are attached to the subject, the comparator triggers a timing circuit that automatically closes Switch S1 and Switch S2 (see Figure 49 for a timing diagram).

These two switches (S1 and S2) enable two different 10 kΩ resistor paths: one between HPSENSE and IAOUT and another between SW and REFOUT. During the time Switch S1 and Switch S2 are enabled, these internal resistors appear in parallel with their corresponding external resistors forming high-pass filters. The result is that the equivalent lower resistance shifts the pole to a higher frequency, delivering a quicker settling time. Note that the fast restore settling time depends on how quickly the internal 10 kΩ resistors of the AD8232 can drain the capacitors in the high-pass circuit. Smaller capacitor values result in a shorter settling time.

If, by the end of the timing, the saturation condition persists, the cycle repeats. Otherwise, the AD8232 returns to its normal operation. If either of the leads off comparator outputs is indicating that an electrode has been disconnected, the timing circuit is prevented from triggering because it is assumed that no valid signal is present. To disable fast restore, drive the FR pin low or tie it permanently to GND.

LEADS OFF DETECTION

The AD8232 includes leads off detection. It features ac and dc detection modes optimized for either two- or three-electrode configurations, respectively.

DC Leads Off Detection

The dc leads off detection mode is used in three-electrode configurations only. It works by sensing when either instrumentation amplifier input voltage is within 0.5 V from the positive rail. In this case, each input must have a pull-up resistor connected to the positive supply. During normal operation, the subject's potential must be inside the common-mode range of the instrumentation amplifier, which is only possible if a third electrode is connected to the output of the right leg drive amplifier.

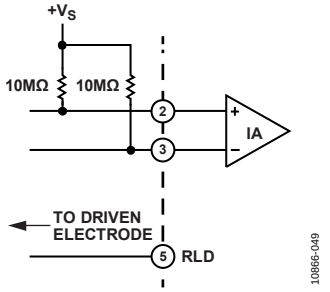

Figure 50. Circuit Configuration for DC Leads Off Detection

Because in dc leads off mode the AD8232 checks each input individually, it is possible to indicate which electrode is disconnected. The AD8232 indicates which electrode is disconnected by setting the corresponding LOD– or LOD+ pin high. To use this mode, connect the AC/$\overline{DC}$ pin to ground.

AC Leads Off Detection

The ac leads off detection mode is useful when using two electrodes only (it does not require the use of a driven electrode). In this case, a conduction path must exist between the two electrodes, which is usually formed by two resistors, as shown in Figure 51.

These resistors also provide a path for bias return on each input. Connect each resistor to REFOUT or RLD to maintain the inputs within the common-mode range of the instrumentation amplifier.

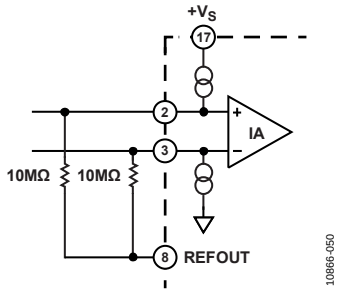

Figure 51. Circuit Configuration for AC Leads Off Detection

The AD8232 detects when an electrode is disconnected by forcing a small 100 kHz current into the input terminals. This current flows through the external resistors from IN+ to IN− and develops a differential voltage across the inputs, which is then synchronously detected and compared to an internal threshold. The recommended value for these external resistors is 10 MΩ. Low resistance values make the differential drop too low to be detected and lower the input impedance of the amplifier. When the electrodes are attached to the subject, the impedance of this path should be less than 3 MΩ to maintain the drop below the comparator's threshold.

As opposed to the dc leads off detection mode, the AD8232 is able to determine only that an electrode has lost its connection, not which one. During such an event, the LOD+ pin goes high. In this mode, the LOD− pin is not used and remains in a logic low state. To use the ac leads off mode, tie the AC/$\overline{\text{DC}}$ pin to the positive supply rail.

Note that while REFOUT is at a constant voltage value, using the RLD output as the input bias may be more effective in rejecting common-mode interference.

STANDBY OPERATION

The AD8232 includes a shutdown pin ($\overline{\text{SDN}}$) that further enhances the flexibility and ease of use in portable applications where power consumption is critical. A logic level signal can be applied to this pin to switch to shutdown mode, even when the supply is still on.

Driving the $\overline{\text{SDN}}$ pin low places the AD8232 in shutdown mode and draws less than 200 nA of supply current, offering considerable power savings. To enter normal operation, drive $\overline{\text{SDN}}$ high; when not using this feature, permanently tie $\overline{\text{SDN}}$ to $+V_S$.

During shutdown operation, the AD8232 is not able to maintain the REFOUT voltage, but it does not drain the REFIN voltage, thereby maintaining this additional conduction path from the supply to ground.

When emerging from a shutdown condition, the charge stored in the capacitors on the high-pass filters can saturate the instrumentation amplifier and subsequent stages. The use of the fast restore feature helps reduce the recovery time and, therefore, minimize on time in power sensitive applications.

INPUT PROTECTION

All terminals of the AD8232 are protected against ESD. In addition, the input structure allows for dc overload conditions that are a diode drop above the positive supply and a diode drop below the negative supply. Voltages beyond a diode drop of the supplies cause the ESD diodes to conduct and enable current to flow through the diode. Therefore, use an external resistor in series with each of the inputs to limit current for voltages beyond the supplies. In either scenario, the AD8232 safely handles a continuous 5 mA current at room temperature.

For applications where the AD8232 encounters extreme overload voltages, such as in cardiac defibrillators, use external series resistors and gas discharge tubes (GDT). Neon lamps are commonly used as an inexpensive alternative to GDTs. These devices can handle the application of large voltages but do not maintain the voltage below the absolute maximum ratings for the AD8232. A complete solution includes further clamping to either supply using additional resistors and low leakage diode clamps, such as BAV199 or FJH1100.

As a safety measure, place a resistor between the input pin and the electrode that is connected to the subject to ensure that the current flow never exceeds 10 μA. Calculate the value of this resistor to be equal to the supply voltage across the AD8232 divided by 10 μA.

RADIO FREQUENCY INTERFERENCE (RFI)

Radio frequency (RF) rectification is often a problem in applications where there are large RF signals. The problem appears as a dc offset voltage at the output. The AD8232 has a 15 pF gate capacitance and 10 kΩ resistors at each input. This forms a low-pass filter on each input that reduces rectification at high frequency (see Figure 53) without the addition of external elements.

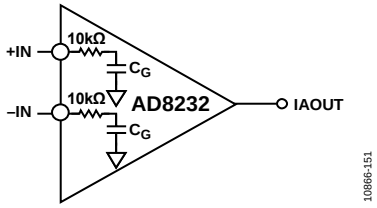

Figure 52. RFI Filter Without External Capacitors

For increased filtering, additional resistors can be added in series with each input. They must be placed as close as possible to the instrumentation amplifier inputs. These can be the same resistors used for overload and patient protection.

POWER SUPPLY REGULATION AND BYPASSING

The AD8232 is designed to be powered directly from a single 3 V battery, such as CR2032 type. It can also operate from rechargeable lithium-ion batteries, but the designer must take into account that the voltage during a charge cycle may exceed the absolute maximum ratings of the AD8232. To avoid damage to the part, use a power switch or a low power, low dropout regulator, such as ADP150.

In addition, excessive noise on the supply pins can adversely affect performance. As in all linear circuits, bypass capacitors must be used to decouple the chip power supplies. Place a 0.1 µF capacitor close to the supply pin. A 1 µF capacitor can be used farther away from the part. In most cases, the capacitor can be shared by other integrated circuits. Keep in mind that excessive decoupling capacitance increases power dissipation during power cycling.

INPUT REFERRED OFFSETS

Because of its internal architecture, the instrumentation amplifier should be used always with the DC blocking amplifier, shown as HPA in Figure 45.

As described in the Theory of Operation section, the dc blocking amplifier attenuates the input referred offsets present at the inputs of the instrumentation amplifier. However, this is true only when the dc blocking amplifier is used as an integrator. In this configuration, the input offsets from the dc blocking amplifier dominate appear directly at the output of the instrumentation amplifier.

If the dc blocking amplifier is used as a follower instead of its intended function as an integrator, the input referred offsets of the in-amp are amplified by a factor of 100.

LAYOUT RECOMMENDATIONS

It is important to follow good layout practices to optimize system performance. In low power applications, most resistors are of a high value to minimize additional supply current. The challenge of using high value resistors is that high impedance nodes become even more susceptible to noise pickup and board parasitics, such as capacitance and surface leakages. Keep all of the connections between high impedance nodes as short as possible to avoid introducing additional noise and errors from corrupting the signal.

To maintain high CMRR over frequency, keep the input traces symmetrical and length matched. Place safety and input bias resistors in the same position relative to each input. In addition, the use of a ground plane significantly improves the noise rejection of the system.

APPLICATIONS INFORMATION

ELIMINATING ELECTRODE OFFSETS

The instrumentation amplifier in the AD8232 is designed to apply gain and to filter out near dc signals simultaneously. This capability allows it to amplify a small ECG signal by a factor of 100 yet reject electrode offsets as large as ±300 mV.

To achieve offset rejection, connect an RC network between the output of the instrumentation amplifier, HPSENSE, and HPDRIVE, as shown in Figure 53.

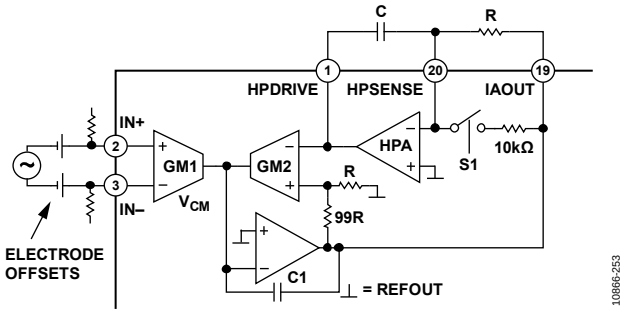

Figure 53. Eliminating Electrode Offsets

This RC network forms an integrator that feeds any near dc signals back into the instrumentation amplifier, thus eliminating the offsets without saturating any node and maintaining high signal gain.

In addition to blocking offsets present across the inputs of the instrumentation amplifier, this integrator also works as a high-pass filter that minimizes the effect of slow moving signals, such as baseline wander. The cutoff frequency of the filter is given by the equation

$$f_{-3dB} = \frac{100}{2\pi RC}$$

where *R* is in ohms and C is in farads.

Note that the filter cutoff is 100 times higher than is typically expected from a single-pole filter. Because of the feedback architecture of the instrumentation amplifier, the typical filter cutoff equation is modified by the gain of 100 of the instrumentation amplifier.

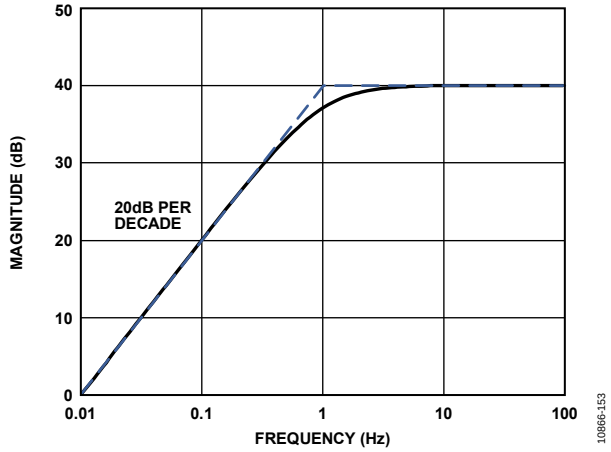

Figure 54. Frequency Response of Single-Pole DC Blocking Circuit

Just like with any high-pass filter with low frequency cutoff, any fast change in dc offset takes a long time to settle. If such change saturates the instrumentation amplifier output, the S1 switch briefly enables the 10 kΩ resistor path, thus moving the cutoff frequency to

$$f_{-3dB} = \frac{100(R+10^4)}{2\pi RC(10^4)} \quad (1)$$

For values of R greater than 100 kΩ, the expression in Equation 1 can be approximated by

$$f_{-3dB} = \frac{1}{200\pi C}$$

This higher cutoff reduces the settling time and enables faster recovery of the ECG signal. For more information, see the Fast Restore Circuit section.

HIGH-PASS FILTERING

The AD8232 can implement higher order high-pass filters. A higher filter order yields better artifact rejection but at a cost of increased signal distortion and more passive components on the printed circuit board (PCB).

Two-Pole High-Pass Filter

A two-pole architecture can be implemented by adding a simple ac coupling RC at the output of the instrumentation amplifier, as shown in Figure 55.

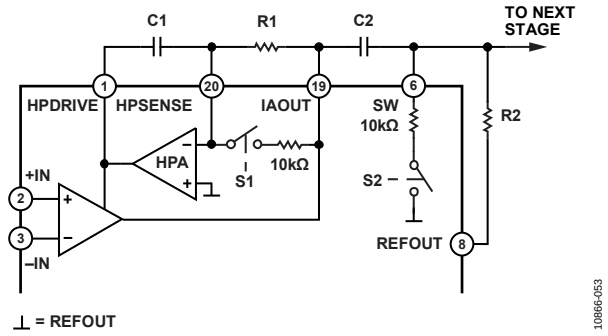

Figure 55. Schematic for a Two-Pole High-Pass Filter

Note that the right side of C2 connects to the SW terminal. Just like S1, S2 reduces the recovery time for this ac coupling network by placing 10 kΩ in parallel with R2. See the Fast Restore Circuit section for additional details on switch timing and trigger conditions.

Keep in mind that if this passive network is not buffered, it exhibits higher output impedance at the input of a subsequent low-pass filter, such as with Sallen-Key filter topologies. Careful component selection can yield good results without a buffer. See the Low-Pass Filtering and Gain section for additional information on component selection.

Additional High-Pass Filtering Options

In addition to the topologies explained in the previous sections, an additional pole may be added to the dc blocking circuit for additional rejection of low frequency signals. This configuration is shown in Figure 56.

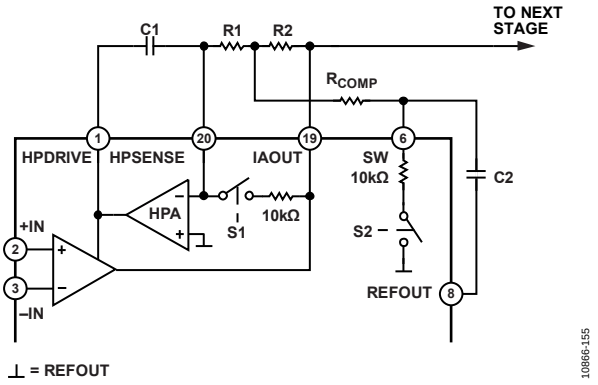

Figure 56. Schematic for an Alternative Two-Pole High-Pass Filter

An extra benefit of this circuit topology is that it allows lower cutoff frequency with lower R and C values and the resistor, R_{COMP}, can be used to control the Q of the filter to achieve narrow band-pass filters (for heart rate detection) or maximum pass-band flatness (for cardiac monitoring).

With this topology, the filter attenuation reverts to a single pole roll off at very low frequencies. Because the initial roll off was 40 dB per decade, this reversion to 20 dB per decade has little impact on the ability of the filter to reject out-of-band low frequency signals.

The designer may choose different values to achieve the desired filter performance. To simplify the design process, use the following recommendations as a starting point for component value selection.

$$R1 = R2 \geq 100\ k\Omega$$

$$C1 = C2$$

$$R_{COMP} = 0.14 \times R1$$

The cutoff frequency is located at

$$f_C = \frac{10}{2\pi\sqrt{R1\ C1\ R2\ C2}}$$

The selection of R_{COMP} to be 0.14 times the value of the other two resistors optimizes the filter for a maximally flat pass band. Reduce its value to increase the Q and, consequently, the peaking of the filter. Keep in mind that a very low value of R_{COMP} can result in an unstable circuit. The selection of values based on these criteria result in a transfer function similar to the one shown in Figure 58.

When additional low frequency rejection is desired, a high-order high-pass filter can be implemented by adding an ac coupling network at the output of the instrumentation amplifier, as shown in Figure 57. The SW terminal is connected to the ac coupling network to obtain the best settling time response when fast restore engages.

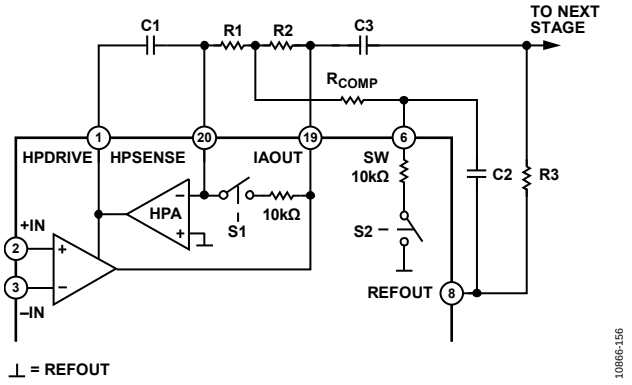

Figure 57. Schematic for a Three-Pole High-Pass Filter

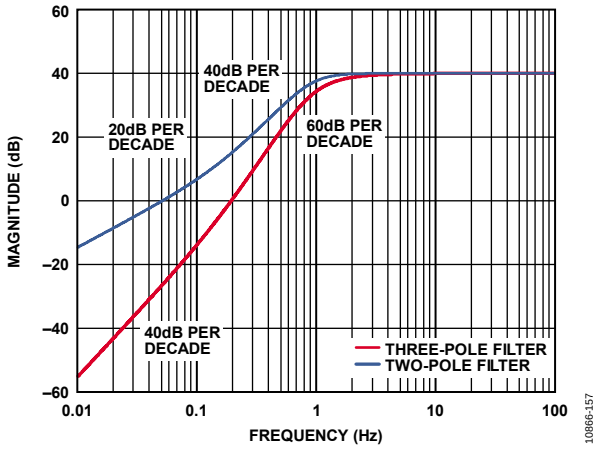

Figure 58. Frequency Response of Circuits in Figure 56 and Figure 57

Careful analysis and adjustment of all of the component values in practice is recommended to optimize the filter characteristics. A useful hint is to reduce the value of R_{COMP} to increase the peaking of the active filter to overcome the additional roll off introduced by the ac coupling network. Proper adjustment can yield the best pass-band flatness.

The design of the high-pass filter involves tradeoffs between signal distortion, component count, low frequency rejection, and component sizes. For example, a single-pole high-pass filter results in the least distortion to the signal, but its rejection of low-frequency artifacts is the lowest Table 4 compares the recommended filtering options.

Table 4. Comparison of High-Pass Filtering Options

	Filter Order	Component Count	Low Frequency Rejection	Capacitor Sizes/Values	Signal Distortion[1]	Output Impedance[2]
Figure 53	1	2	Good	Large	Low	Low
Figure 55	2	4	Better	Large	Medium	Higher
Figure 56	2	5	Better	Smaller	Medium	Low
Figure 57	3	7	Best	Smaller	Highest	Higher

[1] For equivalent corner frequency location.
[2] Output impedance refers to the drive capability of the high-pass filter before the low-pass filter. Low output impedance is desirable to allow flexibility in the selection of values for a low-pass filter, as explained in the Low-Pass Filtering and Gain section.

LOW-PASS FILTERING AND GAIN

The AD8232 includes an uncommitted op amp that can be used for extra gain and filtering. For applications that do not require a high-order filter, a simple RC low-pass filter should suffice, and the op amp can buffer or further amplify the signal.

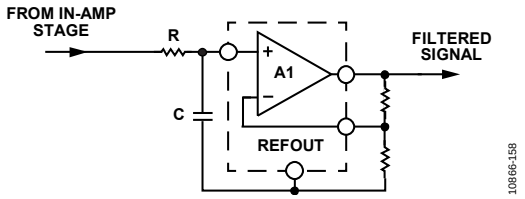

Figure 59. Schematic for a Single-Pole Low-Pass Filter and Additional Gain

Applications that require a steeper roll off or a sharper cut off, a Sallen-Key filter topology can be implemented, as shown in Figure 60.

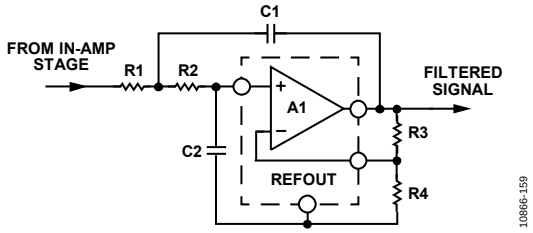

Figure 60. Schematic for a Two-Pole Low-Pass Filter

The following equations describe the low-pass cut off frequency, gain, and Q:

$$f_C = 1/(2\pi\sqrt{(R1\ C1\ R2\ C2)})$$

$$Gain = 1 + R3/R4$$

$$Q = \frac{\sqrt{R1 \times C1 \times R2 \times C2}}{R1 \times C2 + R2 \times C2 + R1 \times C1(1 - Gain)}$$

Note that changing the gain has an effect on Q and vice versa. Common values for Q are 0.5 to avoid peaking or 0.7 for maximum flatness and sharp cut off. A high value of Q can be used in narrow-band applications to increase peaking and the selectivity of the band-pass filter.

A common design procedure is to set R1 = R2 = R and C1 = C2 = C, which simplifies the expressions for cutoff frequency and Q to

$$f_C = 1/(2\pi RC)$$

$$Q = \frac{1}{3 - Gain}$$

Note that Q can be controlled by setting the gain with R3 and R4; however, this limits the gain to be less than 3. For gain values equal to or greater than 3, the circuit becomes unstable. A simple modification that allows higher gains is to make the value of C2 at least four times larger than C1.

It is important to note that these design equations only hold true in the case that the output impedance of the previous stage is much lower than the input impedance of the Sallen-Key filter. This is not the case when using an ac coupling network between the instrumentation amplifier output and the input of the low-pass filter without a buffer.

To connect these two filtering stages properly without a buffer, make the value of R1 at least ten times larger than the resistor of the ac coupling network (labeled as R2 in Figure 55).

DRIVING ANALOG-TO-DIGITAL CONVERTERS

The ability of AD8232 to drive capacitive loads makes it ideal to drive an ADC without the need for an additional buffer. However, depending on the input architecture of the ADC, a simple low-pass RC network may be required to decouple the transients from the switched-capacitor input typical of modern ADCs. This RC network also acts as an additional filter that can help reduce noise and aliasing. Follow the recommended guidelines from the ADC data sheet for the selection of proper R and C values.

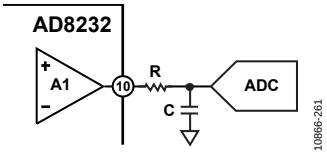

Figure 61. Driving an ADC

DRIVEN ELECTRODE

A driven lead (or reference electrode) is often used to minimize the effects of common-mode voltages induced by the power line and other interfering sources. The AD8232 extracts the common-mode voltage from the instrumentation amplifier inputs and makes it available through the RLD amplifier to drive an opposing signal into the patient. This functionality maintains the voltage between the patient and the AD8232 at a near constant, greatly improving the common-mode rejection ratio.

As a safety measure, place a resistor between the RLD pin and the electrode connected to the subject to ensure that current flow never exceeds 10 μA. Calculate the value of this resistor to be equal to the supply voltage across the AD8232 divided by 10 μA.

The AD8232 implements an integrator formed by an internal 150 kΩ resistor and an external capacitor to drive this electrode. Choice of the integrator capacitor is a tradeoff between line rejection capability and stability. The capacitor should be small to maintain as much loop gain as possible, around 50 Hz and 60 Hz, which are typical line frequencies. For stability, the gain of the integrator should be less than unity at the frequency of any other poles in the loop, such as those formed by the patient's capacitance and the safety resistors. The suggested application circuits use a 1 nF capacitor, which results in a loop gain of about 20 at line frequencies, with a crossover frequency of about 1 kHz.

In a two-lead configuration, the RLD amplifier can be used to drive the bias current resistors on the inputs. Although not as effective as a true driven electrode, this configuration can provide some common-mode rejection improvement if the sense electrode impedance is small and well matched.

APPLICATION CIRCUITS

HEART RATE MEASUREMENT NEXT TO THE HEART

For wearable exercise devices, the AD8232 is typically placed in a pod near the heart. The two sense electrodes are placed underneath the pectoral muscles; no driven electrode is used. Because the distance from the heart to the AD8232 is small, the heart signal is strong and there is less muscle artifact interference.

In this configuration, space is at a premium. By using as few external components as possible, the circuit in Figure 62 is optimized for size.

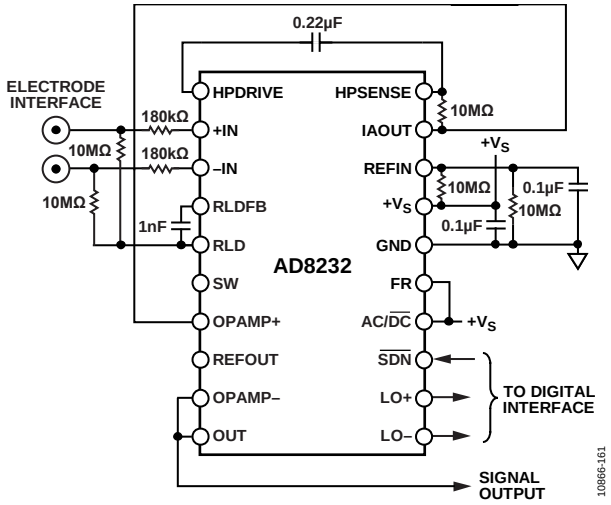

Figure 62. Circuit for Heart Rate Measurement Next to Heart

A shorter distance from the AD8232 to the heart makes this application less vulnerable to common-mode interference. However, since RLD is not used to drive an electrode, it can be used to improve the common-mode rejection by maintaining the midscale voltage through the 10 MΩ bias resistors.

A single-pole high-pass filter is set at 7 Hz, and there is no low-pass filter. No gain is used on the output op amp thereby reducing the number of resistors for a total system gain of 100.

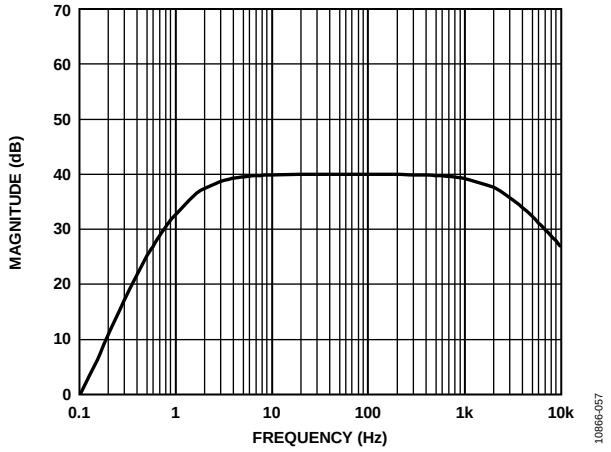

Figure 63. Frequency Response for HRM Next to Heart Circuit

The input terminals in this configuration use two 180 kΩ resistors, to protect the user from fault conditions. Two 10 MΩ resistors provide input bias. Use higher values for electrodes with high output impedance, such as cloth electrodes.

The schematic also shows two 10 MΩ resistors to set the midscale reference voltage. If there is already a reference voltage available, it can be driven into the REFIN input to eliminate these two 10 MΩ resistors.

EXERCISE APPLICATION: HEART RATE MEASURED AT THE HANDS

In this application, the heart rate signal is measured at the hands with stainless steel electrodes. The user's arm and upper body movement create large motion artifacts and the long lead length makes the system susceptible to common-mode interference. A very narrow band-pass characteristic is required to separate the heart signal from the interferers.

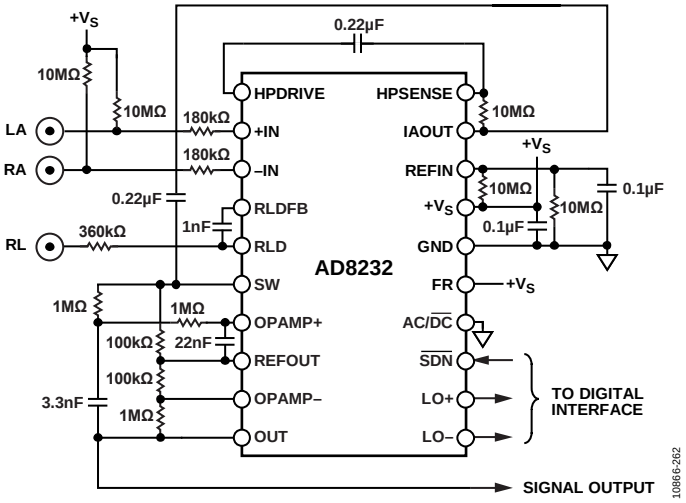

Figure 64. Circuit for Heart Rate Measurement at Hands

The circuit in Figure 64 uses a two-pole high-pass filter set at 7 Hz. A two-pole low-pass filter at 24 Hz follows the high-pass filters to eliminate any other artifacts and line noise.

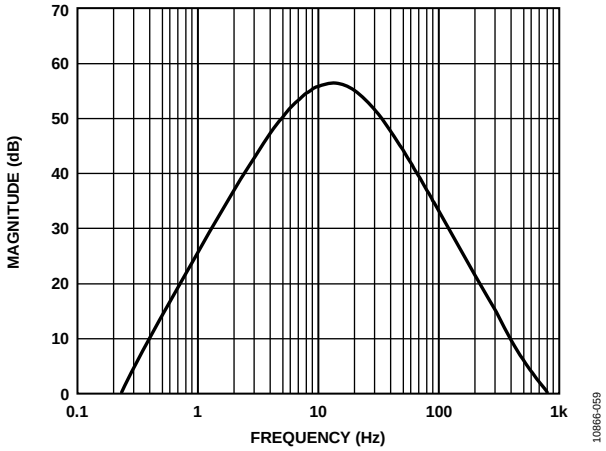

Figure 65. Frequency Response for HRM Circuit Taken at the Hands

The overall narrow-band nature of this filter combination distorts the ECG waveform significantly. Therefore, it is only suitable to determine the heart rate, and not to analyze the ECG signal characteristics.

The low-pass filter stage also includes a gain of 11, to bring the total system gain close to 1100 (note that the filter roll off prevents the maximum gain from reaching this value). Because the ECG signal is measured at the hands, it is weaker than when measured closer to the heart.

The RLD circuit drives to the third electrode, which can also be located at the hands, to cancel common-mode interference.

CARDIAC MONITOR CONFIGURATION

This configuration is designed for monitoring the shape of the ECG waveform. It assumes that the patient remains relatively still during the measurement, and therefore, motion artifacts are less of an issue.

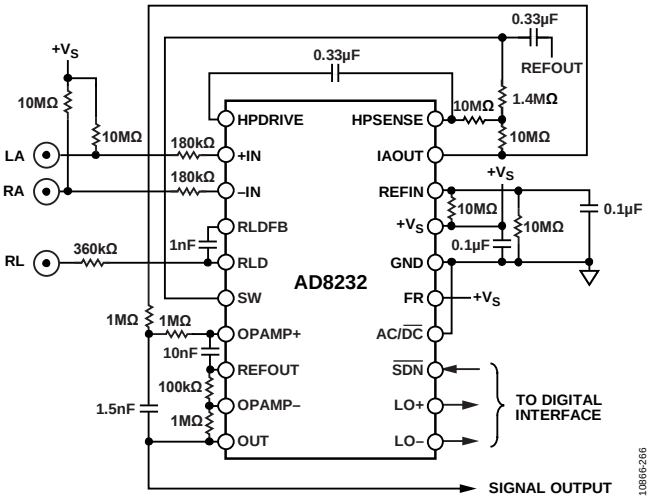

Figure 66. Circuit for ECG Waveform Monitoring

To obtain an ECG waveform with minimal distortion, the AD8232 is configured with a 0.5 Hz two-pole high-pass filter followed by a two-pole, 40 Hz, low-pass filter. A third electrode is driven for optimum common-mode rejection.

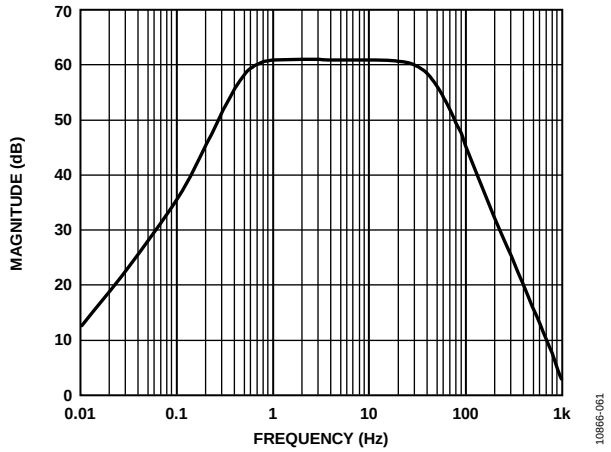

Figure 67. Frequency Response of Cardiac Monitor Circuit

In addition to 40 Hz filtering, the op amp stage is configured for a gain of 11, resulting in a total system gain of 1100. To optimize the dynamic range of the system, the gain level is adjustable, depending on the input signal amplitude (which may vary with electrode placement) and ADC input range.

PORTABLE CARDIAC MONITOR WITH ELIMINATION OF MOTION ARTIFACTS

The circuit in Figure 68 shows an implementation of a battery-powered embedded system for monitoring heart rate in applications where the patient engages in moderate activity, such as with a Holter monitor. The AD8232 uses a three-electrode patient interface and implements a two-pole high-pass filter with a cutoff at 0.3 Hz, and a two-pole low-pass filter with a cutoff frequency of 37 Hz. The total signal gain in the pass band is 400. The fully conditioned signal is sampled by the sigma-delta ADC integrated on the low power microcontroller, ADuCM360. The wide dynamic range of this ADC provides flexibility to reduce the signal gain to avoid saturation, depending on electrode placement.

Because the pass band is relatively wide for ambulatory applications, the ADXL346 accelerometer signal can be used to further minimize the noise introduced by the motion of the patient. Moreover, the microcontroller can use the motion information to monitor inactivity and to issue a system shutdown to save battery power.

The low dropout regulator ensures that the maximum of 3 V is not exceeded, especially during charge cycles of the battery, which can be a lithium-ion cell.

In this application, the ADuCM360 uses its Port 0 to perform DMA transfers to the host communication interface or to an on-board memory, if recording the waveform for later transfer. However, in any particular application, this port should be used for the busiest interface to minimize CPU cycles and maintain low power operation.

Note that this circuit is shown to demonstrate the capabilities of AD8232 and other system components. It is not a complete system design and additional effort must be made to ensure compliance with medical safety guidelines from regulatory agencies.

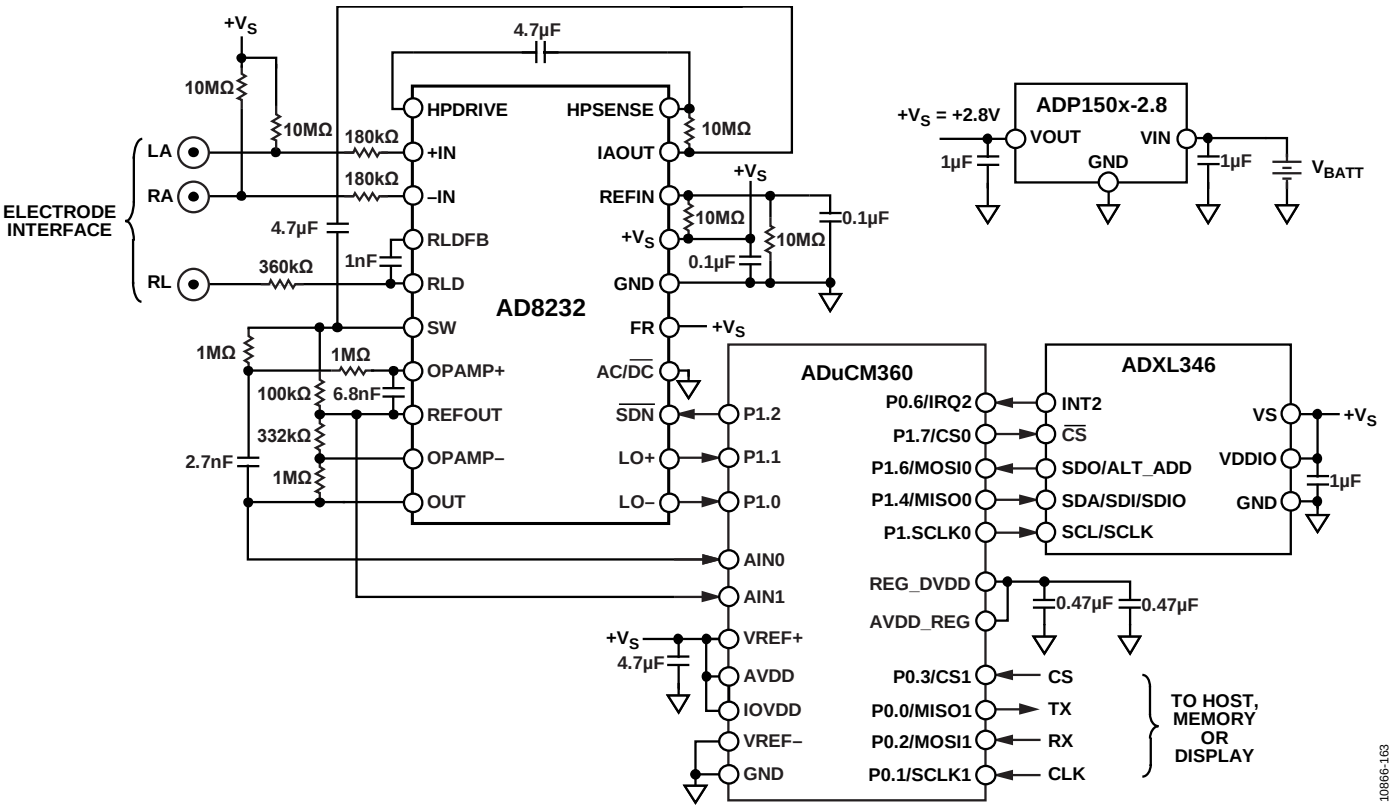

Figure 68. Low Power Portable Cardiac Monitor

PACKAGING AND ORDERING INFORMATION

OUTLINE DIMENSIONS

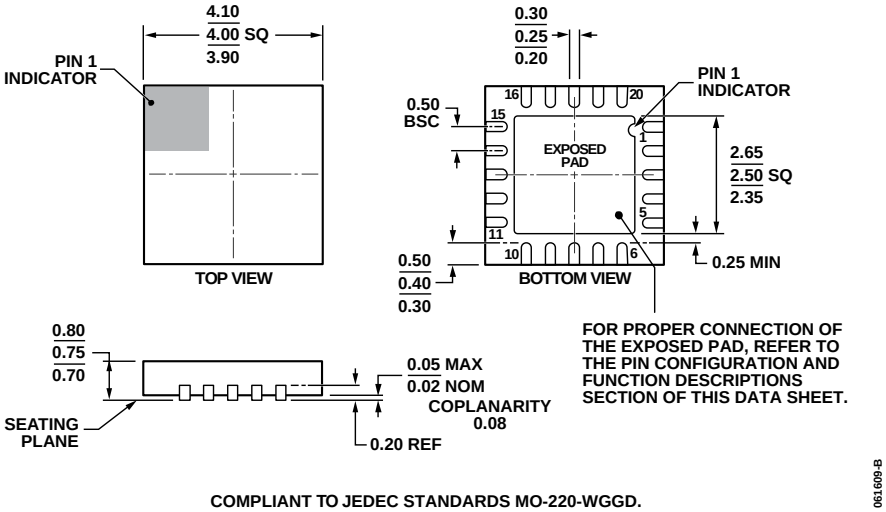

Figure 69. 20-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
4 mm × 4 mm Body, Very Very Thin Quad
(CP-20-10)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD8232ACPZ-R7	−40°C to +85°C	20-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-20-10
AD8232ACPZ-RL	−40°C to +85°C	20-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-20-10
AD8232ACPZ-WP	−40°C to +85°C	20-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-20-10
AD8232-EVALZ		Evaluation Board	

[1] Z = RoHS Compliant Part.

NOTES

D10866-0-2/13(A)