DESIGN OF A SOFT-SWITCHED IBBDAB CONVERTER FOR EV APPLICATIONS

A Project report submitted in partial fulfilment
of the requirements for the degree of B. Tech in Electrical Engineering

By

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CERTIFICATE

To whom it may concern

This is to certify that the project work entitled **'DESIGN OF A SOFT-SWITCHED IBBDAB CONVERTER FOR EV APPLICATIONS'** is the bona fide work carried out by **TAMAGHNA DAS**, University Roll- 11701619036, a student of B. Tech in the Dept. of Electrical Engineering, RCC Institute of Information Technology (RCCIIT), Canal South Road, Beliaghata, Kolkata-700015, affiliated to Maulana Abul Kalam Azad University of Technology (MAKAUT), West Bengal, India, during the academic year 2021-22, in partial fulfilment of the requirements for the degree of Bachelor of Technology in Electrical Engineering and this project has not submitted previously for the award of any other degree, diploma and fellowship.

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It is my great fortune that I have got opportunity to carry out this project work under the supervision of Mr. Sarbojit Mukherjee, Asst. Professor in the Department of Electrical Engineering, RCC Institute of Information Technology (RCCIIT), Canal South Road, Beliaghata, Kolkata-700015, affiliated to Maulana Abul Kalam Azad University of Technology (MAKAUT), West Bengal, India. I express my sincere thanks and deepest sense of gratitude to my guide for his constant support, unparalleled guidance, and limitless encouragement.

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CERTIFICATE of ACCEPTANCE

The report of the Project titled '**Design of a Soft-Switched IBBDAB Converter for EV Applications'** submitted by **TAMAGHNA DAS** (Roll No.: **EE2019/009** of B.Tech. (EE) 8th Semester is hereby recommended to be accepted for the fulfilment of the requirements for B Tech (EE) degree in Maulana Abul Kalam Azad University of Technology.

Name of the Examiner	**Signature with Date**
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i. Abstract

Dual Active Bridge (DAB) converters are widely used in EVs these days. However, the traditional DAB has disadvantages like limited soft-switching range and high currents under wide input voltages. This project incorporates the design of a Bidirectional DAB converter combined with the advantages of a Four-Switch Boost Converter (FSBB). Advantage of the constructed topology is partial sharing of one leg by the two converters, thus reducing the number of switches which further reduces switching and conduction losses. The Integrated Buck-Boost Dual Active Bridge (IBBDAB) converter uses Dual-Edge PWM and Single-Phase-Shift (DE-SPS-PWM) modulation strategies for improved efficiency and high conversion ratio. For low-frequency applications, Zero Voltage Switching (ZVS) for the power switches is easily achieved by the topology.

ii. List of Acronyms

1. *DAB- Dual Active Bridge*
2. *FSBB- Four Switch Buck Boost*
3. *IBBDAB- Integrated Buck Boost Dual Active Bridge*
4. *ZVS- Zero Voltage Switching*
5. *PWM- Pulse Width Modulation*
6. *DE SPS- Dual- Edge Single-Phase-Shifted*
7. *LLC- Inductor-Inductor-Capacitor based Resonant Circuit*
8. *HVDC- High Voltage Direct Current*
9. *MMDC- Multi Modular Direct Current*
10. *MOSFET- Metal Oxide Semiconductor Field Effect Transistor*
11. *EV- Electric Vehicle*

iii. List of Pictures

iv. List of Tables

1. INTRODUCTION

Energy storage devices in EVs which usually consist of batteries and super-capacitors are required for charging and sometimes even reverse charging the DC Bus. However, these ESSs cannot be connected directly to the bus due to voltage mismatch. As solution of this problem, a DC-DC converter can be used in the system. Different types of DC-DC converters [1]–[4] are proposed by different researchers. But after comparing multiple characteristics it has been observed that the bidirectional converters with buck-boost capabilities become most suitable for such application.

2. PROBLEM ANALYSIS

Bidirectional converters can be primarily classified into isolated and non-isolated topologies. The isolated converters are preferred due to their galvanic isolation, high power density, high conversion ratio and high efficiency. Here comes in the DAB topology which has fewer passive components. However, the soft-switching range for DAB converters is very small considering a wide input-voltage condition. Also, under light loading, ZVS is difficult to achieve. For control strategies, dual-phase shift (DPS), triple phase-shift (TPS) and extended phase-shift (EPS) modulation techniques are incorporated but problem lies in their complicacy. The converter built in this project, combines the voltage regulation capability of a FSBB converter with the bidirectional flow characteristic of a DAB converter, that too with reduced number of switches [5]. Moreover, ZVS is easily achieved implementing the DE-SPS-PWM modulation strategy.

3. LITERATURE SURVEY

At present day, a huge variety of converter topologies have gained popularity and different modifications are continuously being made based on their construction or their modulation strategies and so on. Topology wise: [6] drafts a comparison between resonant DC-DC converters that implement an LLC topology and DAB converters when utilized in high-step-conversion-ration applications. The DAB prototype achieves a greater peak efficiency and suffers less losses compared to the LLC prototype at full load condition; In [7], a comparison between multiple modular multilevel DC-DC converters and DAB converters for utilisation in power conversion in HVDC and MVDC. The MMDC and the DAB converters are thoroughly compared in terms of efficiency, count of semiconductor switches and cost of capacitive and magnetic components. It establishes that DAB converters are better than MMDC in many aspects; [8] compares a simple full-bridge forward converter with DAB converter and establishes that the former is better for the said purpose; [9] compares a 2-level PWM to 3-level PWM applicable to DAB converters. It establishes efficiency with two level PWM is higher than three level PWM in the light loads range; While, [10] is an instance where 2-level DAB are compared to multi-level DAB converters, although this project mainly focuses on a 2-level converter. It shows that for the same device-cost, the 2-level DAB outperforms the multi-level DAB, both from an efficiency as well as an operating junction temperature point of view. Therefore, this project is based on a 2-level topology. Phase-shifted control strategies are common for DAB converters. Here, the operation of one H-bridge is phase-shifted from the other. Single, double, triple, and extended phase shifts are common phase-shift models. In [11], detailed comparisons on all different phase-shift modulation techniques implemented in DAB converters, including single, double, triple and extended phase shifts. They study and roughly conclude that EPS is the best strategy for control. Finally, in [12] the study on the estimation of power losses by a DAB converter is described and proposed possible ways to reduce the same. Based on the experiments performed, the estimated power loss is noticed about 4% higher than the measured loss.

4. TOPOLOGY

4.1 Description and Schematics of the IBBDAB Converter

Fig. 1 shows the topology of a typical four-switch buck-boost (FSBB) converter, which is usually adopted under wide input voltage conditions with few components and high gain. Fig. 2 shows the topology of DAB converter. It has similar primary and secondary side full-bridges, a high frequency transformer, an energy transfer inductor, and DC-link capacitors. It has the capability to achieve high conversion ratio and bidirectional power flow. Combining the FSBB converter and DAB converter, the IBBDAB converter is obtained, as shown in Fig. 3. The IBBDAB converter shares the boost leg of FSBB converter with first leg of the DAB converter reducing switches and losses. The IBBDAB converter includes ten switches (Q_1-Q_{10}), a high frequency transformer T, two inductors (L_1, L_2), three resistance-capacitors couples (RC_{in}, RC_o, RC_m) and two voltage sources (V_{in}, V_o). U_c is the voltage across capacitor RC_m. U_{in} is the voltage of input voltage source V_{in}. U_o is the voltage of output voltage source V_o. i_{L1} and i_{L2} are the currents through inductors L_1 and L_2 respectively. u_{ab} is the midpoint voltage of the primary H-bridge. u_{cd} is the midpoint voltage of the secondary H-bridge. i_c is the output current of FSBB converter.

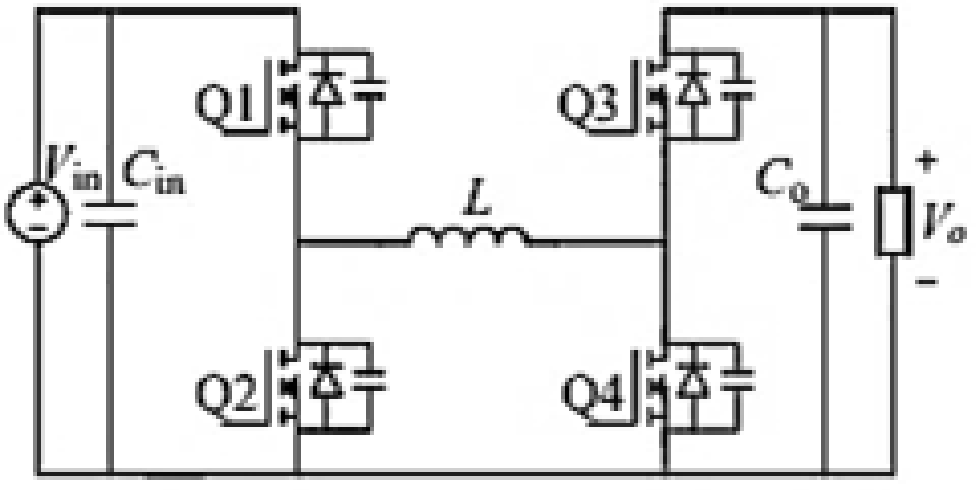


Fig 1: FSBB Converter

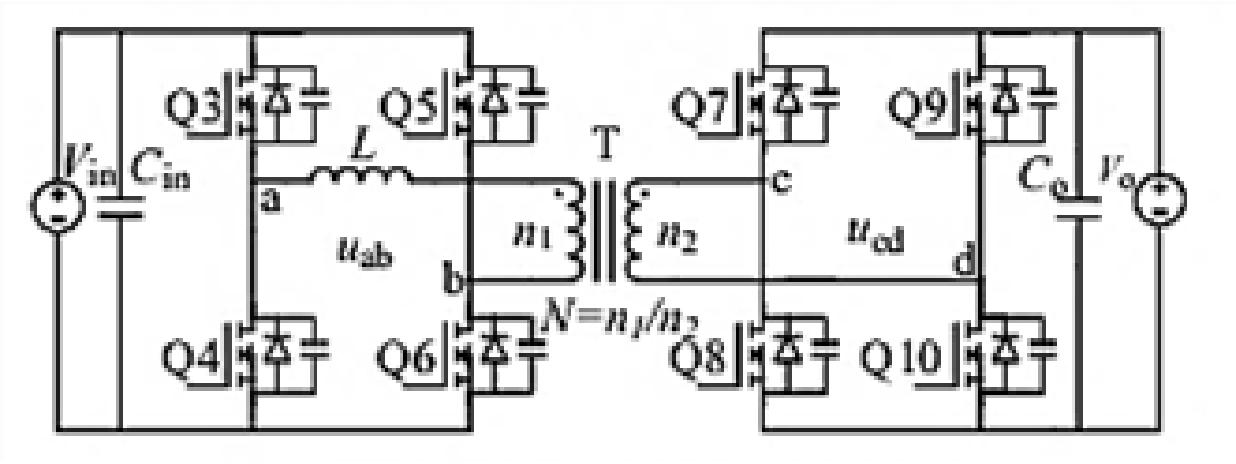


Fig 2: DAB Converter

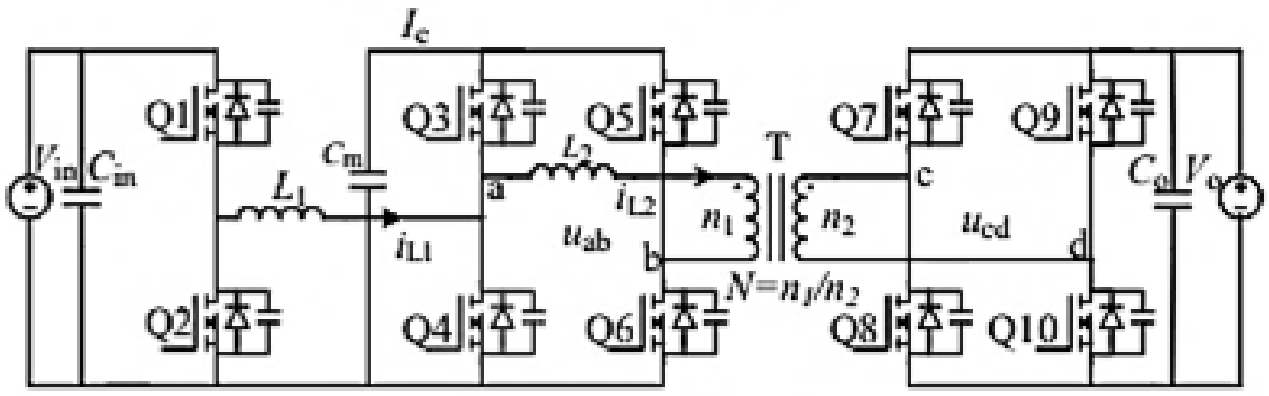


Fig 3: Schematic of IBBDAB Converter

4.2 Gain of the IBBDAB Converter

The gain of FSBB converter is written as-

$$M_1 = \frac{d_1}{1 - d_2} \tag{1}$$

where d_1 and d_2 are the duty cycle of Q_1 and Q_4. The gain of DAB converter is expressed as-

$$M_2 = N = \frac{n_1}{n_2} \tag{2}$$

where N is the turns ratio of transformer, n_1 and n_2 are the primary and secondary turns of transformer.
Therefore, the gain of IBBDAB converter is obtained as-

$$M = \frac{M_1}{M_2} = \frac{d_1}{(1 - d_2)N} \tag{3}$$

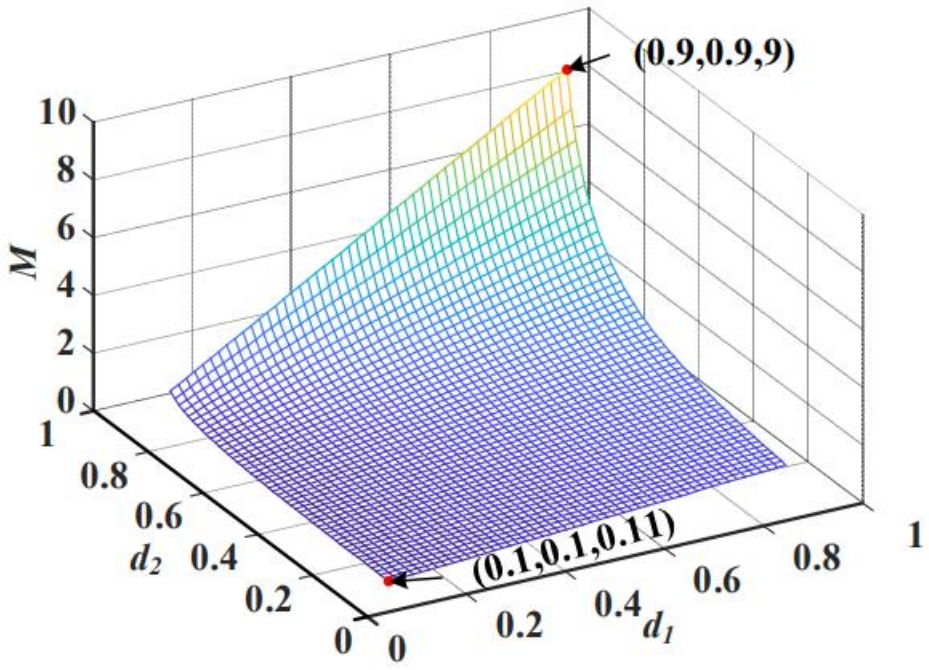


Fig 4: Converter Gain

Supposing N=1, the voltage regulation capability of the IBBDAB converter can be achieved. The value of d1 is between 0.1 and 0.9. The value of d2 is between 0.1 and 0.9. The value of M is between 0.11 and 9. Hence, the proposed converter is able to work in step-up or step-down, which makes the optimization of the DAB converter easier especially under wide input voltage.

4.3 Modulation Strategy of the IBBDAB Converter

Single-phase-shift (SPS) is a typical modulation strategy with simple control and convenient implementation, which has been widely used in DAB converter. Thanks for the voltage regulation capability of FSBB converter, the highvoltage side and the low-voltage side of DAB converter can be easily matched. By adopting the SPS modulation strategy, the current stress of the DAB converter is greatly reduced and the soft-switching range gets an obvious expansion.

There are two common modulations for the FSBB converter: dual-edge modulation and constant-frequency zero-voltage-switching (CF-ZVS) modulation. CF-ZVS modulation needs to detect the zero-crossing point accurately and carefully config the value of the inductor. Besides, the soft-switching range is sensitive to the load. Compared with CF-ZVS modulation, dual-edge modulation is more convenient to implement and achieve high efficiency. This modulation can significantly reduce the ripple and root-meansquare values of inductor current. Therefore, this paper prefers the dual-edge PWM modulation for the FSBB converter.

The dual-edge PWM plus SPS (DE-PWM-SPS), which consists of SPS and dual-edge modulation, is finally selected for IBBDAB converter. Dual-edge modulation is more convenient to implement and achieve high efficiency. This modulation can significantly reduce the ripple and root-mean-square values of inductor current. By adopting the SPS modulation strategy, the current stress of the DAB converter is greatly reduced and the soft-switching range gets an obvious expansion. For this project, the duty cycle of Q_3 and Q_4 is fixed at 0.5. Then, the gain M can be expressed as-

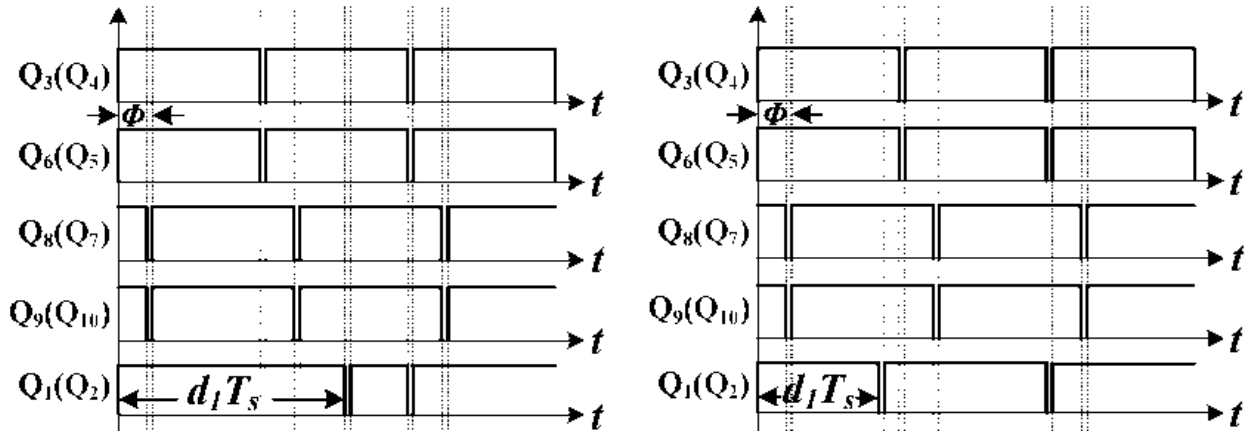
$$M = \frac{2d_1}{N} \tag{4}$$

4.4 Principle of Operation of the IBBDAB Converter

d_1 is the duty cycle of Q_1 which can regulate the input voltage into a constant voltage. Φ is the phase shift between primary H-bridge and secondary H-bridge of DAB converter, which can be utilized to control the power flow in both directions.

The IBBDAB converter can work in step-up or step-down modes. Combining the DE-PWM-SPS modulation with the converter, the operating modes can be further explained in terms of the duty cycle of switch Q_1. When the duty cycle of switch Q_1, $d_1 > 0.5$, the converter works in step-up mode. While, $d_1 < 0.5$ makes the converter work in step-down mode. Fig-5 shows the switching strategies as implemented in the converter.

Fig-5 shows the switching strategies of switches Q_1 – Q_{10} during buck and boost modes respectively.



(a) Boost Mode **(b) Buck Mode**

Fig 5: Switching Strategies of Q_1 – Q_{10}

5. SIMULATION

5.1 Simulation Diagram

Fig. 6 shows the simulation diagram of the IBBDAB converter. It comprises of 10 MOSFETs and a single high frequency isolation transformer along with filters at both, source, and load ends. The hardware construction of the traditional DAB is underway. Once functional, the 2 extra switches meant for the integrated buck-boost capability will be incorporated and their pulses configured. Q_1 and Q_2 have complementary operation.

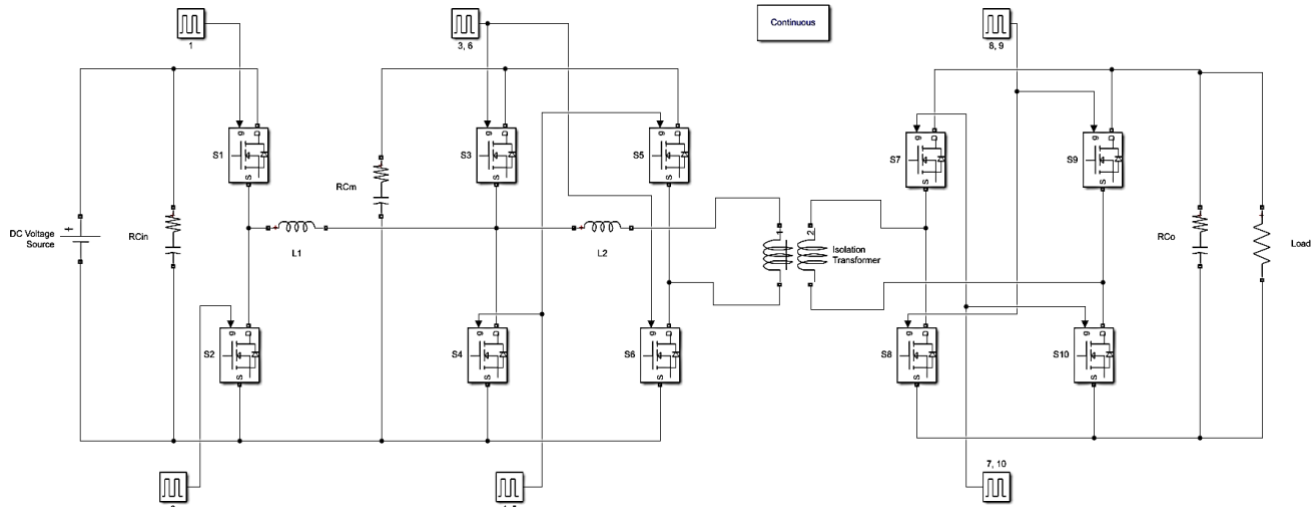


Fig 6: Simulation diagram of IBBDAB converter

5.2 Component Details

Table-1 mentions the specifications of all components used in the simulation circuit. Also, the safe operating frequency for achieving soft-switching is found to be up to 10kHz.

The gate-drivers are built using FAN7392N ICs that have a characteristic, in-built, dead-time calculation, and incorporation feature. The switches that will be used in the hardware are IRF540 N-channel MOSFETs. The MOSFET drivers are designed to be a powered by a single 220V-15V-2A transformer which will have 5 tappings at its secondary, each of which while power one leg.

Parameter	Element	Value
Rated Input Voltage	U_{in}	24V
Rated Output Voltage	$U_{o\,(peak)}$ (boost)	48V
	$U_{o\,(peak)}$ (buck)	5V
Rated Power	-	20W
Inductance	L_1	400µH
	L_2	400µH
Capacitance	C_{in}	300µF
	C_m	1000µF
	C_o	1000µF
Operating Frequency	f_s	10kHz

Table 1. Component Details

6. HARDWARE MODEL

The hardware model of the IBBDAB converter consists of 3 major parts, viz., the gate drivers for the converter switches which make up the control circuit, the converter itself, constituting the power circuit and the central isolating transformer.

i. **IBBDAB Converter-** The analysis of the converter using simulation has been fully achieved. However, due to component unavailability and funding issues, the full-fledged working prototype of the converter has not yet been completed. The feasible part of the converter is built using IRF540N N-channel MOSFETs. The inductors, L_1 and L_2, have been designed. Input, middle and output filters as well as the snubber circuits are yet to be realized in hardware. The isolation transformer must be a customised 1:3 ratio transformer with calculated core.

ii. **Power Supply-** The Drain and Source of two corresponding MOSFETs of each leg are connected to the DC voltage that is to be manipulated, stepped up or down. In prototype, this power source is realized in a single 220V-24V-5A transformer, which, through the converter, can drive a load of 30W. The terminals of the transformer are further connected to a rectifier circuit that converts the 24V AC into DC. This DC voltage is further regulated using a dedicated voltage regulator IC and an RC filter before finally supplying it to the converter.

iii. **Gate Drivers-** The gate drivers are designed using FAN7392N ICs which work like any other typical drivers like the IR2110 or the DGD0506, but incorporate an extra dead-time calculation and application feature without further complication of the circuit.

(a) These 5 driver ICs will require a power supply of 5V at their VDD (9) pin to power up.
(b) To supply the MOSFETs, the ICs are also to be powered at their VCC pin (3). This will be provided using a single 220V-12V-2A transformer whose secondary will be tapped to give 5 isolated outputs, one for each driver.
(c) The brain of the circuit lies in an STM-32 G474 development board which is coded accordingly to output 10 sets of Dual-Edge Single-Phase-Shifted PWM, viz., 5 signals in pairs of complements.
(d) Each pair of complementary PWM is supplied to the HIN and LIN pins of the FAN7392N IC respectively.
(e) The FAN IC drives the gate of the MOSFETs to output said amount of voltage as stated by the PWM signal.

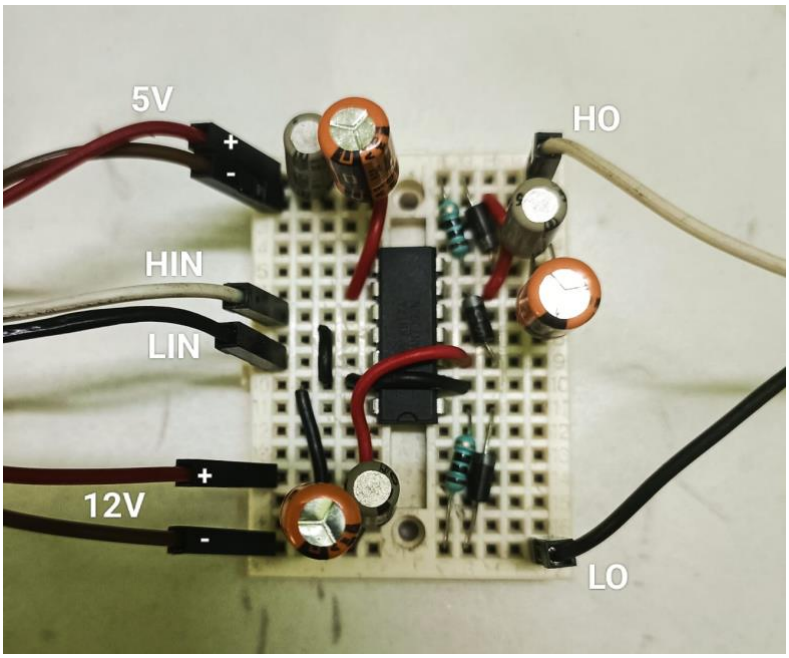
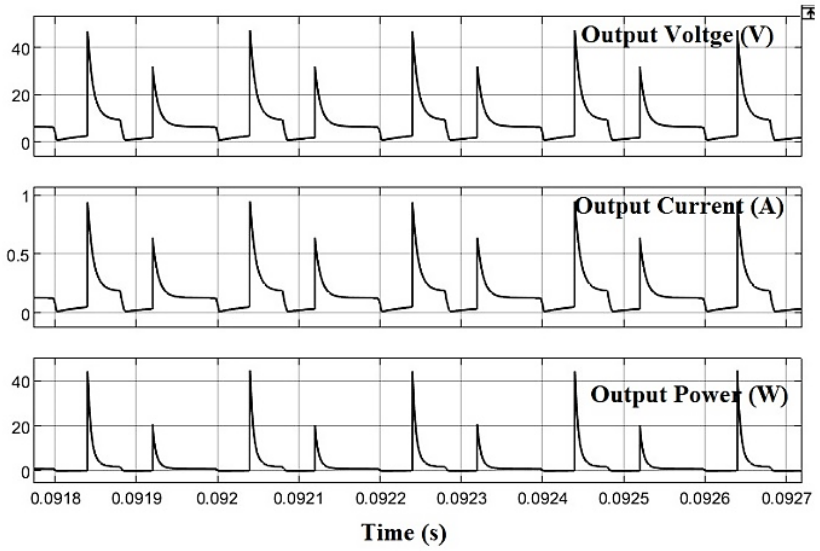


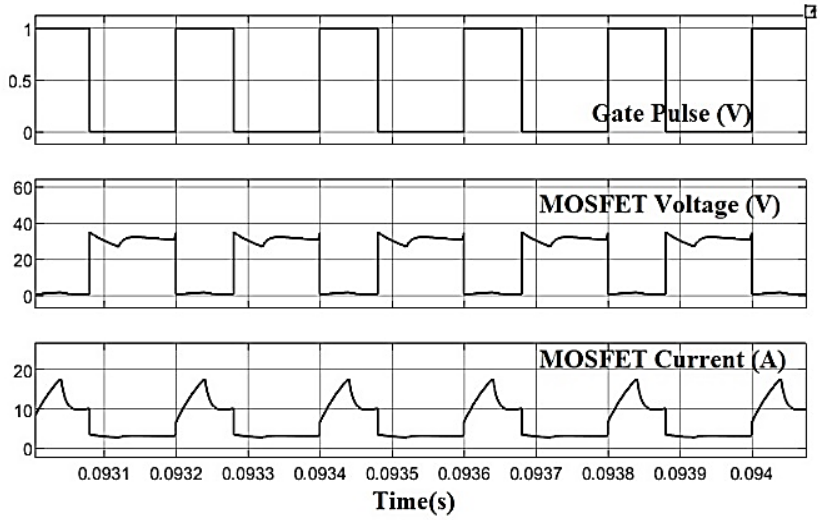
Fig- MOSFET Gate Driver using FAN7392 (centre IC)

7. OBSERVATIONS AND RESULTS

The simulation was run in buck and boost modes. Fig. 7 shows the output parameters and switch parameters of the IBBDAB in boost mode, while Fig. 8 shows the same for buck mode. In both cases, the input voltage is taken to be 24V. In boost mode, a peak output voltage of 48V with a current of 0.9A is observed as shown in Fig. 7(a). Similarly, in buck mode, a peak voltage of 15V along with peak current of 0.32A is observed as shown in the Fig. 8(a). The soft-switching of the DAB converter switches are also established in the Fig. 7(b) and Fig. 8(b). So, reduction of switching loss is sucessfully achieved.

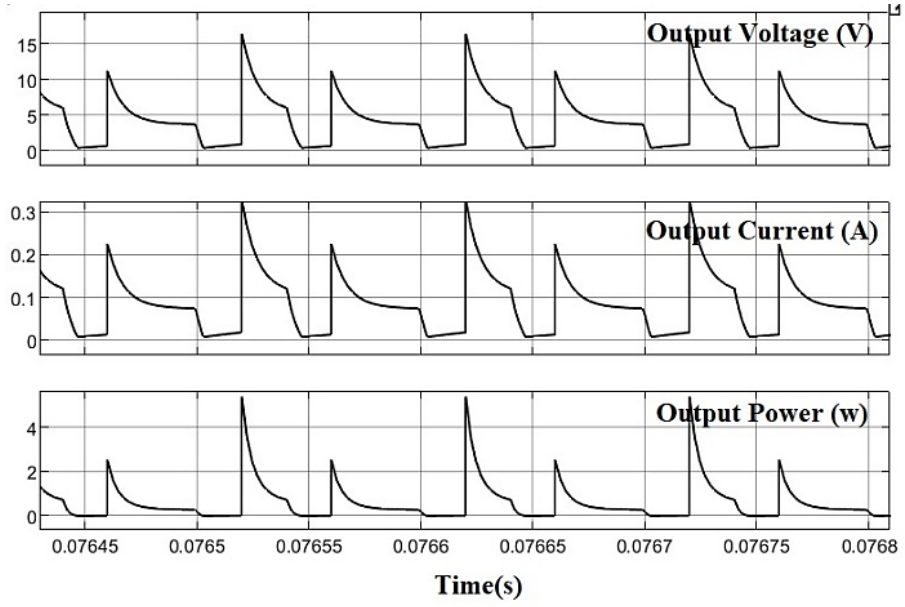


(a)

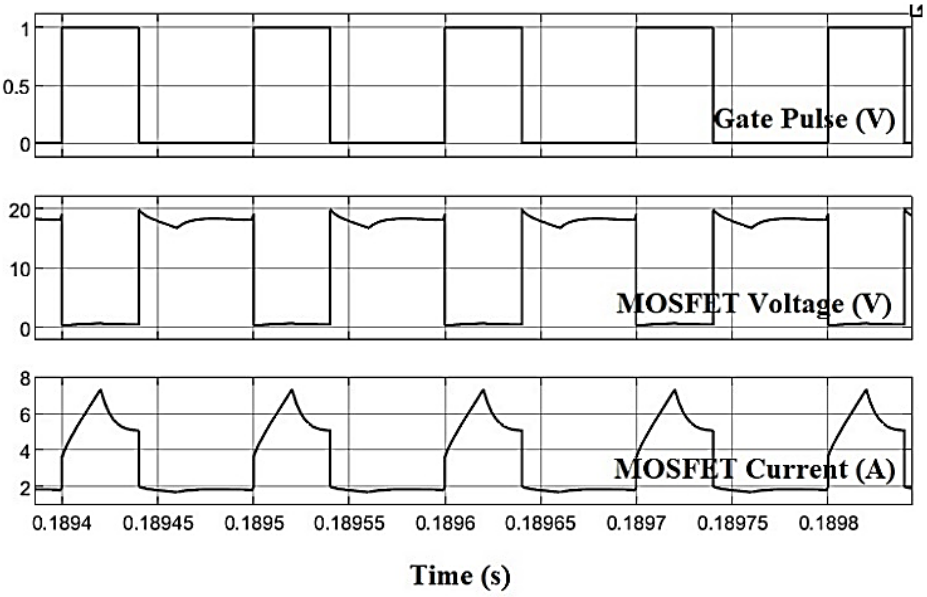


(b)

Fig 7: Boost Mode: (a) Output voltage, current and power (b)MOSFET gate pulse, voltage, current



(a)



(b)

Fig 8: Buck Mode: (a) Output voltage, current and power
(b) MOSFET gate pulse, voltage, current

8. COMPARISON

A rough comparison is made between the topology used in this project with other different infamous topologies. It is found after comparison that, although the number of power switches is more, the advantages that the IBBDAB converter has over other topologies overcomes its only demerit, thereby concluding its effectiveness and efficiency.

Topology	**Number of H.V. switches**	**Switch Stress**	**Operating power range for max. efficiency**	**Buck-Boost Capability**	**Soft-switching capability**	**Control**
Multi-Modular DC	Variable	High	Medium	No	NA	Hard-Switching
LLC Resonant	2	Low	Low	No	Good	Frequency Control
Traditional DAB	2	High	High	No	Good	Phase-Shift PWM
IBBDAB	10	Low	All	Yes	Very good	Single Phase-Shifted Dual-Edge PWM

Table 2. Comparison Table

9. COST ANALYSIS

Sl No.	Component	Cost (Real/Estimate-INR)
1.	Resistors*	40/-
2.	Capacitors*	30/-
3.	Inductors*	1500/-
4.	Diodes*	50/-
5.	MOSFET Switches	300/-
6.	FAN7392N MOSFET Driver	275/-
7.	Wires	60/-
8.	Transformer-1	375/-
9.	Transformer-2	120/-
10.	STM-32 G474	3000/-
Total		**5730/-**

*Prices are inclusive of all components from all parts of the project for resistors, capacitors and inductors- including the actual converter, its snubber circuits, gate drivers, etc.

Thereby, making the cost analysis, we can interpret that a converter of this efficiency and effectiveness can be realized within a very small size and will cost much lesser than one built using a different topology. If instead of the STM32 controller board, only the processor mounted on it is used, the price will be further reduced, thus allowing the cost of the converter circuit to be almost half of other topologies.

10. FUTURE WORK

The project aims to build a converter with high conversion ratio as well as bidirectional capabilities. Once constructed, this converter can be used to: (i) Charge EVs from a wide range of input voltages or in fact reverse charge the DC bus; (ii) Coupled with inverter topologies, it can be used to design a microgrid that will convert renewable energy sources like wind and solar into electrical energy with high efficiency.

11. CONCLUSION

In this project, the FSBB and DAB converters are studied and their advantages are coupled into a novel IBBDAB converter. The IBBDAB increases the soft-switching range and the DE-SPS-PWM largely reduces circulating currents. Switches are reduced due to sharing of legs. Analysis of the output voltage-current graphs obtained, show achievement of ZVS, and the converter gain shown in eqn. (4) is clarified.

12. REFERENCES

[1] K. Sayed, E. H. El-Zohri, and H. Mahfouz, "Analysis and design for interleaved ZCS buck DC-DC converter with low switching losses," *International Journal of Power Electronics*, vol. 8, no. 3, pp. 210–231, 2017, doi: 10.1504/IJPELEC.2017.085076.

[2] S. Mukherjee, "A SEPIC-Cuk-CSCCC Based SIMO Converter Design Using PSO-MPPT For Renewable Energy Application," *Journal of Electrical and Computer Engineering Innovations*, vol. 10, no. 2, pp. 437–446, 2022, doi: 10.22061/JECEI.2022.8379.509.

[3] S. Mukherjee, S. S. Saha, and S. Chowdhury, "Design of duty-ratio and phase-shift control circuits for MPPT of SPV Source using ZV-ZCS PSFB Converters," in *Proceedings of 4th International Conference on 2021 Devices for Integrated Circuit, DevIC 2021*, 2021, pp. 555–559, doi: 10.1109/DevIC50843.2021.9455893.

[4] S. Mukherjee, C. Mal, and G. Yadav, "Design of MPPT DC-DC Converter Fed Ripple Switch Inductor Quasi-ZSI with Different Control Methods For Renewable Energy Application," *Neuro Quantology*, vol. 20, no. 9, pp. 4715–4726, 2022, doi: 10.14704/nq.2022.20.9.NQ44547.

[5] C. Xu *et al.*, "A Novel Converter Integrating Buck-Boost and DAB Converter for Wide Input Voltage," *IECON Proceedings (Industrial Electronics Conference)*, vol. 2020-October, pp. 2877–2882, 2020, doi: 10.1109/IECON43393.2020.9254322.

[6] S. Mukherjee, A. Kumar, and S. Chakraborty, "Comparison of DAB and LLC DC-DC Converters in High-Step-Down Fixed-Conversion-Ratio (DCX) Applications," *IEEE Transactions on Power Electronics*, vol. 36, no. 4, pp. 4383–4398, 2021, doi: 10.1109/TPEL.2020.3019796.

[7] S. P. Engel, M. Stieneker, N. Soltau, S. Rabiee, H. Stagge, and R. W. De Doncker, "Comparison of the modular multilevel DC converter and the dual-active bridge converter for power conversion in HVDC and MVDC grids," *IEEE Transactions on Power Electronics*, vol. 30, no. 1, pp. 124–137, 2015, doi: 10.1109/TPEL.2014.2310656.

[8] L. Roggia, F. Beltrame, L. Schuch, and J. R. Pinheiro, "Comparison between full-bridge-forward converter and DAB converter," *2013 Brazilian Power Electronics Conference, COBEP 2013 - Proceedings*, pp. 224–229, 2013, doi: 10.1109/COBEP.2013.6785119.

[9] K. Kusaka, S. Member, and J. Itoh, "Comparison of two level PWM and three level PWM in Dual Active Bridge converter," *2016 IEEE International Conference on Sustainable Energy Technologies (ICSET)*, pp. 311–314, 2016, doi: 10.1109/ICSET.2016.7811801.

[10] B. Alikhanzadeh, A. Bahmani, and T. Thiringer, "Efficiency investigation of 2L-DAB and ML-DAB for high-power PV applications," *2018 13th International Conference on Ecological Vehicles and Renewable Energies, EVER 2018*, pp. 1–6, 2018, doi: 10.1109/EVER.2018.8362340.

[11] A. Kumar, A. H. Bhat, and P. Agarwal, "Comparative analysis of dual active bridge isolated DC to DC converter with single phase shift and extended phase shift control techniques," *2017 6th International Conference on Computer Applications in Electrical Engineering - Recent Advances, CERA 2017*, vol. 2018-January, pp. 397–402, 2018, doi: 10.1109/CERA.2017.8343363.

[12] Y. H. Abraham, H. Wen, W. Xiao, and V. Khadkikar, "Estimating power losses in Dual Active Bridge DC-DC converter," *2011 2nd International Conference on Electric Power and Energy Conversion Systems, EPECS 2011*, pp. 1–5, 2011, doi: 10.1109/EPECS.2011.6126790.

[13] S. Mukherjee, S. S. Saha, and S. Chowdhury, "Design of duty-ratio and phase-shift control circuits for MPPT of SPV Source using ZV-ZCS PSFB Converters," *in Proceedings of 4th International Conference on 2021 Devices for Integrated Circuit, DevIC 2021*, 2021, pp. 555–559, doi: 10.1109/DevIC50843.2021.9455893.

[14] S. Mukherjee, "A SEPIC-Cuk-CSCCC Based SIMO Converter Design Using PSO-MPPT For Renewable Energy Application," *Journal of Electrical and Computer Engineering Innovations,* vol. 10, no. 2, pp. 437–446, 2022, doi: 10.22061/JECEI.2022.8379.509.

APPENDIX A

A.1 Specifications of Hardware Components

(i) IRF540N N-Channel MOSFET

Parameter	Symbol	Value	Units
Drain-Source Voltage	V_{DSS}	100	V
Drain-Gate Voltage	V_{DGR}	100	V
Gate-Source Voltage	V_{GS}	± 20	V
Power Dissipation	P_D	120	W
Operating Temperature	T_J	-55 to 175	°C

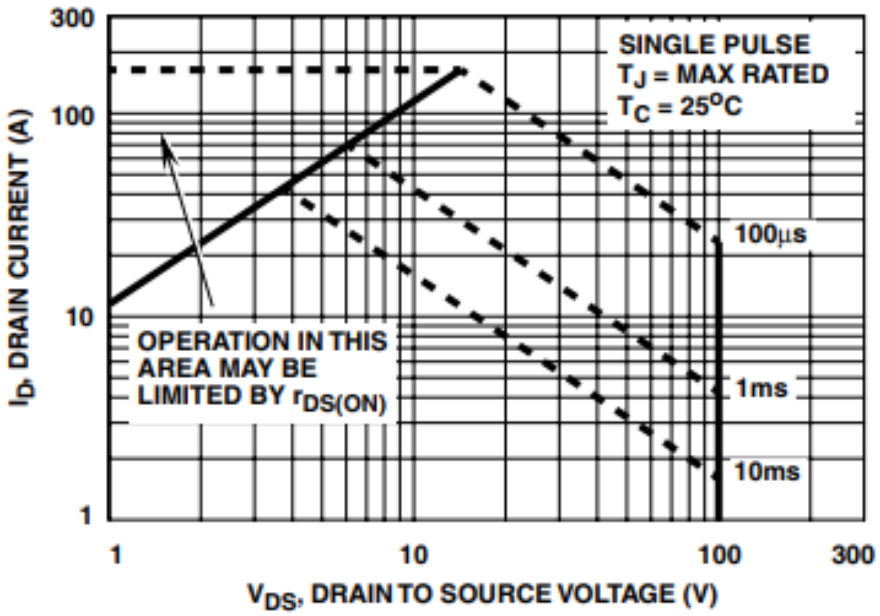


Fig- Forward Bias Characteristics of IRF540N

(ii) FAN7392N N-Channel MOSFET Driver

Parameter	Symbol	Value	Units
Turn-on Propagation Delay	$t_{PD(ON)}$	130-180	ns
Turn-off Propagation Delay	$T_{PD(OFF)}$	150-200	ns
Turn-on Rise Time	t_{rise}	25-50	ns
Turn-off Fall Time	t_{fall}	20-45	ns
Operating Temperature	T_A	40-80	°C
Input Current at V_{DD}		10-120	μA
Input Current at V_{CC}		40-430	μA
Input Voltage	V_{DD}	3	V
	V_{CC}	15	V
	V_{HIN}	2.4	V
	V_{LIN}	9.5	V
Ouput Voltage	V_{HO}	1.5	V
	V_{LO}	200	mV

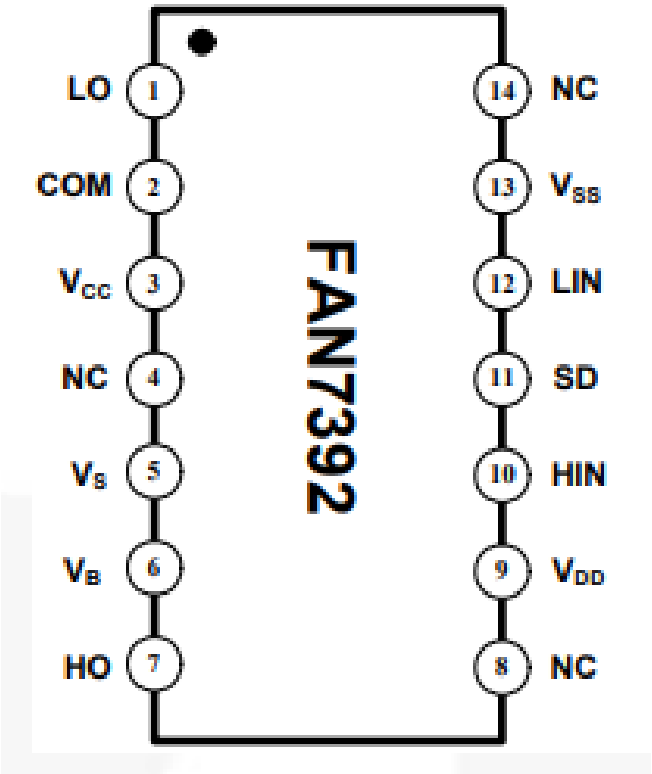


Fig- 14 DIP FAN7392N N-Channel MOSFET IC

(Top View)

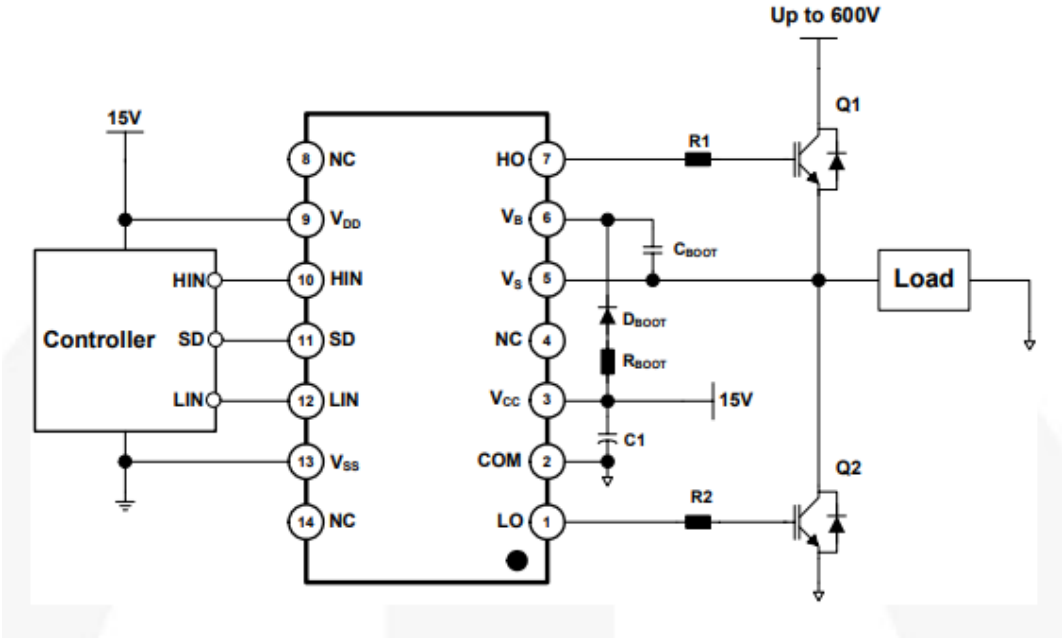


Fig- Typical Application Diagram of FAN7392N Driver IC

iii. STM-32 G474 Development Board

Parameter	Specifications
Processor	ARM Cortex- M33 Core
Memory	1MB flash; 128KB SRAM
Connectivity	SCI * 6, I^2C * 2, SPI, etc.
Pins	ADC12 * 2, DAC12 * 2, Temperature Sensor
Timers	32-bit * 4, 16-bit * 4, AGT * 6
Working Frequency	8-24 MHz
Operating Voltage	2.7 - 3.6 V
Operating Temperature	-40°C to 85°C

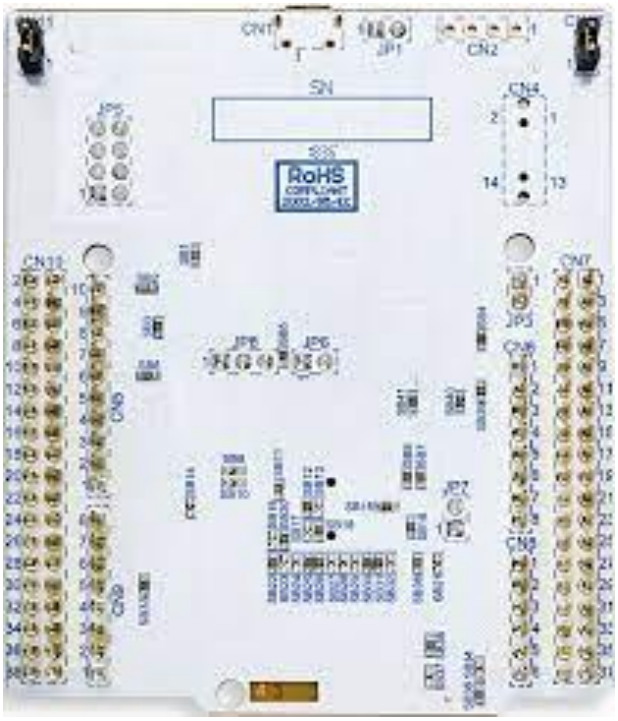


Fig- STM32 G474 Development Board

iv. Central Transformer*[1]

Undersaid are the design considerations for the 1:3 ratio based transformer that provides galvanic isolation to the entire circuit.

$V_P = 150V;$

$V_S = 48V;$

$f_{SW} = 10kHz;$

$P_s = 50W$

$P_{avg} = (50 + 50\sqrt{2})/2$

$= 60.355W$

$\approx 60W$

$I_S = P_S/V_S$

$= 50/48$

$= 1.0416A$

Considering a cosmo core,

$A_P = (P_{avg} * 10^4) / (2 * f * B_m * K_f * K_w * K_j)$

$= 1.33cm^4$

$N_P = (V_P * 10^3) / (4 * f * B_m * A_c)$

$= 39.164$

≈ 40 turns

$N_S = (V_P / V_S) * N_S$

$= 125$ turns

$I_P = I_S * (N_S/N_P)$

$= 3.255A$

$a_{CP} = I_P / 3$

$= 1.085\ mm^2$

$a_{CS} = I_S / 3$

$= 0.3472\ mm^2$

From SWG chart we find, 22 SWG wires have a cross-section of 0.3973mm^2. If a triple core 22 SWG is considered, the final c.s. results to 1.919mm^2 which meets the requirement of 1.085mm^2 minimum c.s. area for carrying the primary current.

again, from SWG chart we find, 27 SWG wires have a C.S. of 0.1363mm^2. If a triple core 27 SWG is used, the final C.S. results to 0.4089mm^2 which meets the requirement of 1.0416mm^2 C.S. area for carrying the secondary current.

Therefore, for the purpose of central transformer, the transformer specifications are as follows-

Core: 0.250 E-I cosmo core

Primary: 3-core 22 SWG – 40 turns

Secondary: 3-core 27 SWG – 120 turns

*[1] For COSMO core transformers, the values of the constants are-

$K_w = 0.3$

$K_i = 300$

$K_f = 1$

$B_m = 0.25$

Design and Dimensional Data for Three Phase Laminations

The dimensional outline for 3Phase EI laminations and an assembled transformer is shown in Figure 3-26. Dimensional data for 3Phase EI laminations is given in Table 3-10; design data is given in Table 3-11.

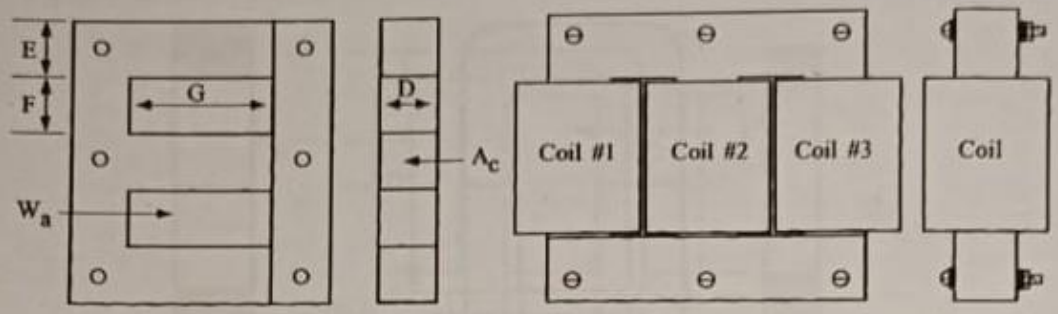


Figure 3-26. EI Three Phase Laminations Outline.

Table 3-10. Dimensional Data for 14 mil EI Three Phase Laminations.

3Phase, Standard Laminations, Thomas & Skinner 14 mil									
Part No.	D cm	E cm	F cm	G cm	Part No.	D cm	E cm	F cm	G cm
0.250EI	0.635	0.635	0.871	2.858	1.000EI	2.540	2.540	3.810	7.620
0.375EI	0.953	0.953	1.270	3.175	1.200EI	3.048	3.048	3.048	7.620
0.500EI	1.270	1.270	1.588	3.493	1.500EI	3.810	3.810	3.810	9.525
0.562EI	1.427	1.427	1.588	5.398	1.800EI	4.572	4.572	4.572	11.430
0.625EI	1.588	1.588	1.984	5.634	2.400EI	6.096	6.096	6.096	15.240
0.875EI	2.223	2.223	2.779	6.111	3.600EI	9.144	9.144	9.144	22.860

Table 3-11. Design Data for 14 mil EI Three Phase Laminations.

3Phase, Standard Laminations, Thomas & Skinner 14 mil									
Part No.	W_{cu} grams	W_{tfe} grams	MLT cm	W_a / $2A_c$	A_c cm^2	W_a cm^2	A_p cm^4	K_g cm^5	A_t cm^2
0.250EI	57	54	4.3	3.251	0.383	2.49	1.43	0.051	53
0.375EI	134	154	6.2	2.339	0.862	4.03	5.21	0.289	102
0.500EI	242	324	8.2	1.810	1.532	5.54	12.74	0.955	159
0.562EI	403	421	8.8	2.213	1.936	8.57	24.88	2.187	207
0.625EI	600	706	10.1	2.334	2.394	11.18	40.13	3.816	275
0.875EI	1255	1743	13.9	1.809	4.693	16.98	119.53	16.187	487
1.000EI	2594	2751	16.7	2.368	6.129	29.03	266.91	39.067	730
1.200EI	2178	3546	17.6	1.316	8.826	23.23	307.48	61.727	725
1.500EI	4266	6957	22.0	1.316	13.790	36.29	750.68	187.898	1132
1.800EI	7326	12017	26.3	1.316	19.858	52.26	1556.61	470.453	1630
2.400EI	17230	28634	34.8	1.316	35.303	92.90	4919.66	1997.995	2899
3.600EI	58144	96805	52.2	1.316	79.432	209.03	24905.75	15174.600	6522

v. Inductors Design Analysis*[2]

Undermentioned are the design considerations of the two inductors, viz, L_1 and L_2.

$L = 400\ \mu H$; $I_P = 3.255A$; $I_{rms} = 1.0416$

Considering a ferrite core,

$A_P = [\ (L * I_P * I_{rms} * 10) / (B_m * K_w * K_j)\ ]^{(1/1+x)}$

$= 0.2224\ cm^4$

$N = (L * I_P * 10^4) / (B_m * A_C)$

$= 149.65$ turns

≈ 150 turns

Now,

$a_{CS} = I_{rms} / 3$

$= 0.3472\ mm^2$

From SWG chart we find, 21 SWG wires have a cross-section of $0.5189\ mm^2$. If a triple core 21 SWG is considered, the final C.S. will be enough to carry the currents for each inductor.

Therefore, for the purpose of both inductors, the specifications are as follows-

Core: EE-2425 ferrite core

Coil: 3-core 21 SWG – 150 turns

*[2] For Ferrite core transformers, the values of the constants are-

$K_w = 0.3$

$K_i = 630$

$K_f = 1$

$B_m = 0.25$

Design and Dimensional Data for EE Ferrite Cores

The dimensional outline for EE ferrite cores is shown in Figure 3-30. Dimensional data for EE ferrite cores is given in Table 3-18; design data is given in Table 3-19.

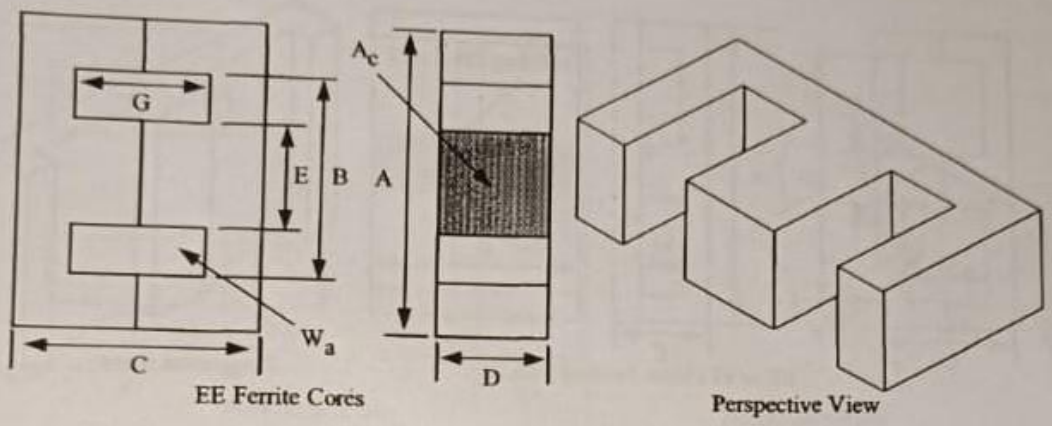


Figure 3-30. Dimension Outline for EE Ferrite Cores.

Table 3-18. Dimensional Data for EE Ferrite Cores.

EE, Ferrite Cores (Magnetics)													
Part No.	A cm	B cm	C cm	D cm	E cm	G cm	Part No.	A cm	B cm	C cm	D cm	E cm	G cm
EE-187	1.930	1.392	1.620	0.478	0.478	1.108	EE-21	4.087	2.832	3.300	1.252	1.252	2.080
EE-2425	2.515	1.880	1.906	0.653	0.610	1.250	EE-625	4.712	3.162	3.940	1.567	1.567	2.420
EE-375	3.454	2.527	2.820	0.935	0.932	1.930	EE-75	5.657	3.810	4.720	1.880	1.880	2.900

Table 3-19. Design Data for EE Ferrite Cores.

EE, Ferrite Cores (Magnetics)											
Part No.	W_{icu} grams	W_{ife} grams	MLT cm	MPL cm	W_a/A_c	A_c cm^2	W_a cm^2	A_p cm^4	K_g cm^5	A_t cm^2	*AL mh/1K
EE-187	6.8	4.4	3.8	4.01	2.219	0.228	0.506	0.116	0.0028	14.4	500
EE-2425	13.9	9.5	4.9	4.85	2.068	0.384	0.794	0.305	0.0095	23.5	767
EE-375	36.4	33.0	6.6	6.94	1.875	0.821	1.539	1.264	0.0624	45.3	1167
EE-21	47.3	57.0	8.1	7.75	1.103	1.490	1.643	2.448	0.1802	60.9	1967
EE-625	64.4	103.0	9.4	8.90	0.808	2.390	1.930	4.616	0.4700	81.8	2767
EE-75	111.1	179.0	11.2	10.70	0.826	3.390	2.799	9.487	1.1527	118.0	3467

*This AL value has been normalized for a permeability of 1K. For a close approximation of AL for other values of permeability, multiply this AL value by the new permeability in kilo-perm. If the new permeability is 2500, then use 2.5.